Influence of the poly gate depletion effect on programming EEPROM cells

F. Schuler, P. Klein*, K. Hoffmann, O. Kowarik

University of Bundeswehr Munich, ET4, Werner-Heisenberg-Weg 39, D-85577 Neubiberg,
phone: +49/89/6004-3662, fax: -2223, Franz.Schuler@unibw-muenchen.de
*Siemens AG, Balanstr. 73, D-81541 Munich,
phone: ++49/89/636-22952, fax: -23147,Peter.Klein@hl.siemens.de

I. Introduction

It is known from literature (fig. 1) [1] that the data retention decreases drastically if the doping concentration of the floating gate (FG) N_{FG} is increased. Unfortunately a low doping concentration causes a non-negligible voltage drop across the FG. This effect is known by MOS transistors [2] and can be explained by the formation of a depletion region (DR) in the poly silicon. To our knowledge this effect has not been considered so far by EEPROM models e.g. [3]. This voltage drop across the FG reduces the FN-programming efficiency and the V_T shift seriously.

II. Measurement, Simulation and Discussion

Applying a positive voltage at the control gate (CG) depletion regions in the CG itself and in the FG will be created. The voltage drop across the depletion region depends on the doping levels. Because of the larger effective oxide thickness d_i^{eff} between the CG and the FG resulting from the ONO-structure the voltage drop in the CG can be neglected contrary to the one in the FG (fig. 2a).

According to the subcircuit (fig. 2b) with the 3 connected capacitances a programming voltage of

$$\Phi_t = V_{CG} \frac{C_i'}{C_i' + C_t} \tag{1}$$

$$C_i' = \frac{C_i C_d}{C_i + C_d} \tag{2}$$

results.

The value of the depletion capacitance

$$C_d = A \sqrt{\frac{q \epsilon_0 \epsilon_{poly}}{2 \Phi_d} N_{FG}} \tag{3}$$

depends strongly on the doping concentration N_{FG} and the voltage Φ_d across it .

Measuring the capacitances of a test stucture with a contacted FG (fig. 3) the floating gate doping concentration N_{FG} near the interface can be determined. Evaluation of measured capacitances of quarter micron test structures results in an average poly gate doping concentration of $N_{FG} = 5 \cdot 10^{19} \mathrm{cm}^{-3}$.

It is obviously that if the depletion capacitance C_d is not considered the calculated programming voltage will be larger than the expected one. Thus the real tunnel current

$$I_{tunnel} = -B_1 \frac{\Phi_t}{d_t} \exp\left(-\frac{B_2}{\Phi_t / d_t}\right) \tag{4}$$

will be much smaller than the calculated one.

To further verify this effect device simulations (MEDICI) have been performed on an EEPROM cell with a tunnel oxide thickness of 6 nm and a variable doping concentration of the FG. The programming has been simulated by a CG voltage ramp of 0.2 ms, a maximal CG voltage of 12 V and a total programming time of 0.5 ms. The results are shown in fig. 4 and fig. 5: The lower the doping concentration the larger is the voltage drop Φ_d across the FG and the lower the resulting tunnel current.

According to the tunnel current performance the charge on the FG can be determined as a function of time and doping concentration as parameter (fig. 6). For a given ΔV_T of e.g. 1V the programming time as a function of doping concentration can be extracted (fig. 7). For a fixed programming time one can observe a linear dependence of the lost of the V_T-shift and the poly gate doping concentration (fig. 8).

III. Conclusion

To ensure data retention of 10 years there is a maximum allowed poly gate doping concentration. It has been shown that the poly doping concentrations of typical quarter micron processes result in a ΔV_T-lost of more than $1V$ affected by the poly gate depletion effect. Therefore a compromise has to be choosen between required data retention and programming performance. This is particularly important if a high resolution as e.g. in multi level storage is required.

This work was sponsored by the DFG (Ho 1325/2-2).

References

[1] H. Watanabe et al., Symposium on VLSI Technology Digest of Technical Papers 1994, p. 47
[2] N. D. Arora et al., ED-42, No. 5, May 1995
[3] Luey Chwan Liong et al., ED-40, No. 1, Jan. 93

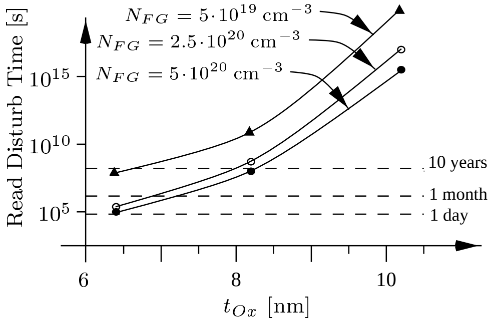

Fig. 1: The read disturb time of EEPROM cells after 10^6 W/E stress cycles according to [1].

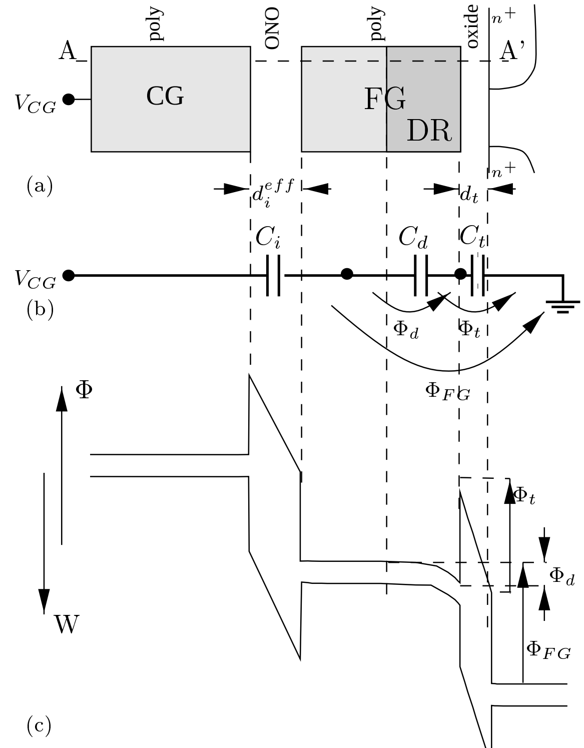

Fig. 2: a) Cross-section of EEPROM,
b) Equivalent circuit: cross-section A-A'
c) Valence and conduction band

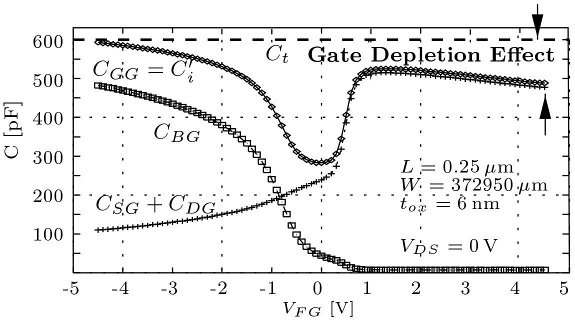

Fig. 3: Capacitances behaviour of a quarter micron test structure demonstrating the influence of the poly gate depletion effect.

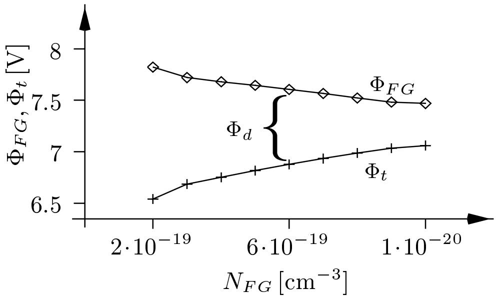

Fig. 4: Programming voltage (Φ_t), floating gate voltage (Φ_{FG}) and voltage drop across depletion region (Φ_d) as functions of the poly gate doping concentration.

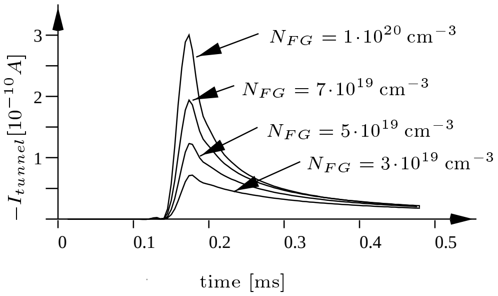

Fig. 5: Tunnel current as a function of time for different poly gate doping concentrations.

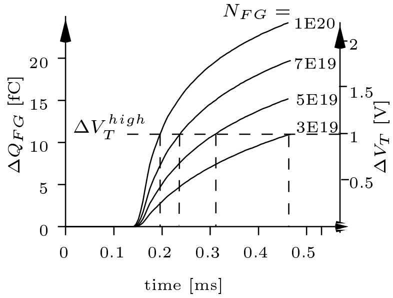

Fig. 6: Charging of the FG and the resulting V_T-shift as a function of time and the poly gate doping concentration N_{FG} as parameter.

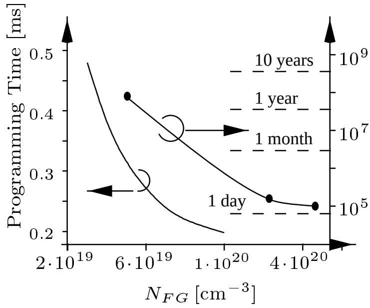

Fig. 7: Programming time required to reach a V_T-shift of 1V and data disturb time according to [1] as functions of the poly gate doping N_{FG}.

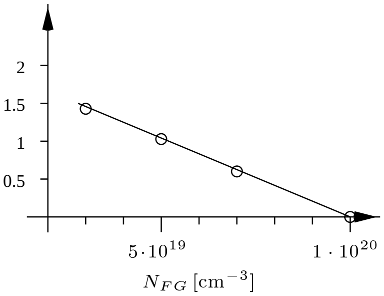

Fig. 8: ΔV_T-lost for different poly gate doping concentrations and a programming time of 0.5 ms.