High Speed Capacitive Coupled Interface for Multipoint Connections

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Abstract

A capacitivly coupled interface for a bidirectional data bus like a Controller-DRAM-bus with data transfer rates up to 1Gb/s at a power supply voltage of 1.5V is presented. All receivers are capacitively coupled to the data bus. The CMOS receiver consumes 1.65mW DC-power in a 0.35μm technology. The computed power consumption of the driver for a bus with five I/Os is reduced approximatly to $\frac{1}{4}$ and to $\frac{1}{8}$ in comparison with a SSTL (Stub Series Terminated Logic) system and a RSL (Rambus Signaling Logic) system at a transfer rate of 1Gb/s respectively.

1. Introduction

To implement a high speed Controller-DRAM-bus in a low power application it is necessary to optimize the system's bandwidth and its power consumption. Both depend mainly on the interconnect length, the parasitics, the driver resistance, and the termination of the data bus. In general a higher bandwidth or a higher transfer rate leads to higher power consumption. A high speed system needs a termination resistor to reduce reflections on the busline. This resistor adds a DC-path to the system which increases the power consumption. The RDRAM-system (Rambus - a RSL system [2]) and the SLDRAM-system (Synclink - a SSTL system [3]) are two examples for this kind of high speed data bus. These are the two systems with the highest transfer rate at this time. To avoid the DC-path there are some solutions with dynamic termination publicated [1] but only for lower transfer rates. A bus system with capacitive coupled interface (CCI) eleminates the system's DC-path and consumes less power at the same transfer rate than RDRAM and SLDRAM.

2. Conception of the CCI

Fig. 1 shows the Controller-DRAM-busses for SLDRAM and RDRAM in the case that the controller drives the busline. Every busline has it's termination resistor R_{tt} on one end which connects the busline to the termination voltage V_{tt} (V_{DD} for the RSL). The SSTL-bus has serial resistors R_s between the busline and the I/O to reduce the reflections on the busline. Best results for

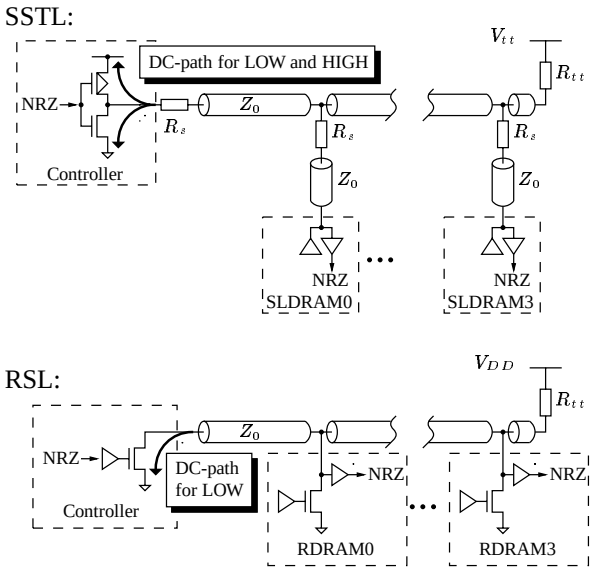

Figure 1. SSTL- and RSL-Controller-DRAM-bus

the SSTL-50Ω-bus are obtained with a serial resistor of 25Ω. Because of the high ohmic input resistance of the reciever/transmitter the RSL bus gets small reflection coefficients on the busline and does not need serial resistors to damp the occuring reflections. Both interfaces transfer Non-Return-to-Zero (NRZ) signals in a Dual Data Rate. The driver of the SSTL-interface consumes DC-power for both states HIGH and LOW because the line's termination voltage V_{tt} is defined as $\frac{V_{DD}}{2}$ and so there is always a DC-current flowing through the driver resistor. The driver of the RSL-interface allows a DC-path only at the LOW state when the open-drain output driver pulls actively down the voltage level on the busline.

The CCI-Controller-DRAM-bus and it's transmission mode is shown in Fig. 2. Every I/O of the CCI has a coupling capacitance C_k in serial to it's link to the busline. Due to this capacitance the NRZ signal on the driver's output gets differentiated. The differentiation of the positive edge generates a positive peak on the busline, the negative edge a negative one. The peaks occur only when the driver changes it's output state. The positive peak sets the receiver's output to a HIGH signal which is stored. The negative peak resets the output to a LOW

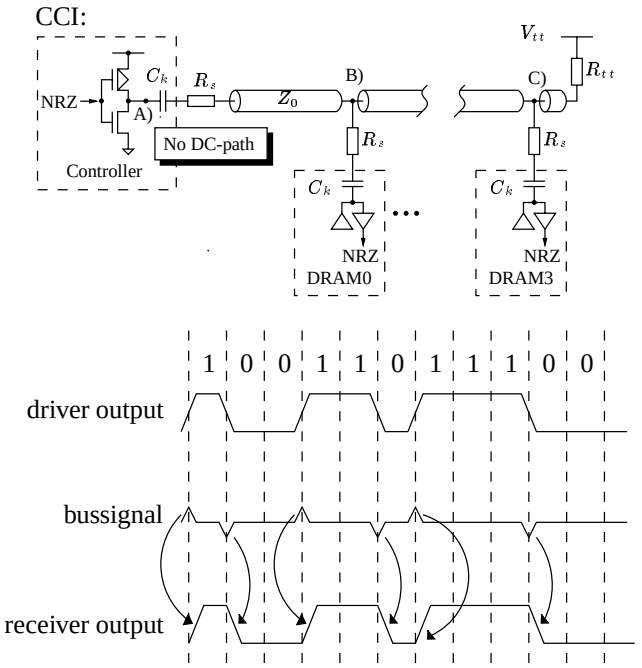

Figure 2. CCI-Controller-DRAM-bus and the CCI transmission mode

signal. The NRZ signal is regenerated at the receiver's output. The CCI-bus has no DC-path and therefore no DC-power-dissipation. Since every I/O causes a non zero reflection coefficient on the busline, the CCI-bus needs serial resistors R_s in serial to the coupling capacitance to avoid oscillations on it. To demonstrate the influence of R_s on the performance of the CCI-system two examples for the value of R_s are described:

a) $R_s = 25\Omega$: the highest possible signal amplitude is achieved with a serial resistor of 25Ω. For lower values of R_s the system becomes instable. Reflections occuring on the busline are gated with a receiver circuit having the trip points above and below the occuring reflections.

b) $R_s = 75\Omega$: the system's bandwidth is reduced to avoid ringing on the busline. Due to this the signal amplitude gets smaller and the reflections do not cause major over- and undershoots because they occur at the falling and rising edge of the bussignal.

With the above values of R_s a CCI-bus with five I/Os, a parasitic bond inductance L_p of 2.5nH, a pad capacitance C_p of 4pF and a coupling capacitance C_k of 1.5pF is simulated. Fig. 3 shows the signals at node A), B) and C) for both cases.
After a power up the receiver needs an external RESET signal to have a defined output state. Apart from that RESET signal the CCI works with the protocol of Rambus and Synclink respectively. So only few modifications on the protocols are necessary to install a CCI in a RDRAM-bus and a SLDRAM-bus environment

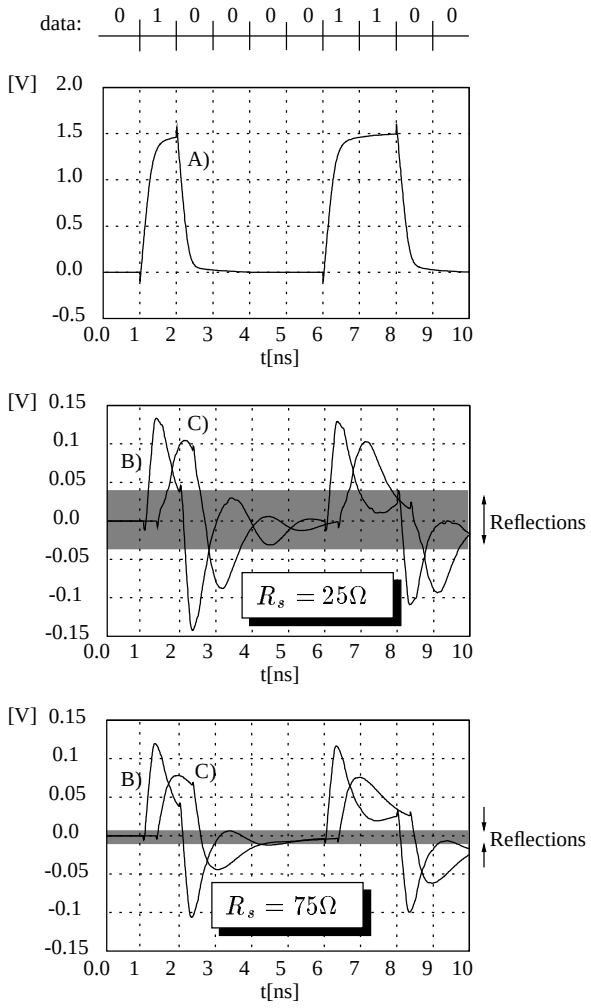

Figure 3. Simulated signals at node A), B) and C) (Fig. 2) for $R_s = 25\Omega$ and $R_s = 75\Omega$

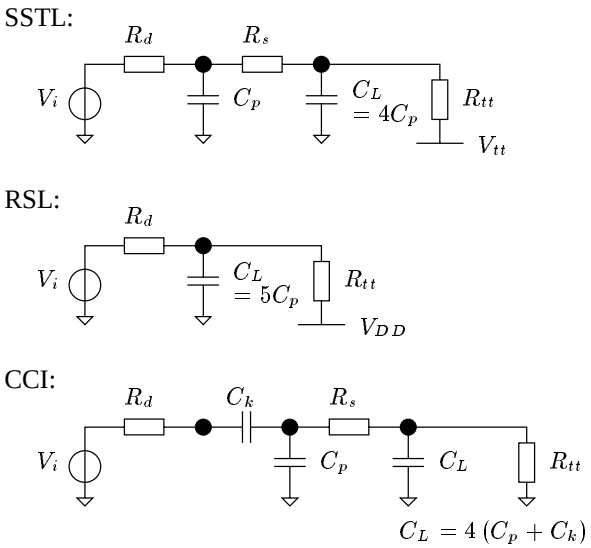

Figure 4. Equivalent circuits

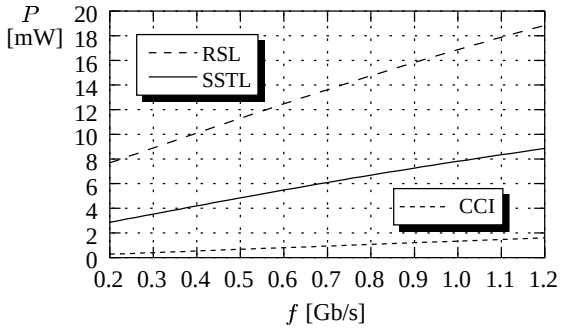

Figure 5. Driver power as a function of transfer rate for V_{DD} =1.5V in each case

3. Driver Power Consumption

The driver power consumption of RSL, SLDRAM and CCI is computed as a function of the transfer rate for a data burst of alternating 1-0 at a supply voltage of 1.5V (Fig. 5). The basic of every calculation is an equivalent circuit for a 50Ω-bus with five I/Os shown in Fig. 4. The values of the network elements are

$R_d = 30\Omega$	$R_s = 25\Omega$	$R_{tt} = 25\Omega$
$C_p = 4$pF	$C_k = 1.5$pF	$V_i = 0$V / 1.5V

The parasitic inductance is omitted because it's influence is negligible. The driver is presented as a voltage source V_i with a constant output resistor R_d. The conclusion is that the power consumption for driving the CCI-system is approximately $\frac{1}{4}$ and $\frac{1}{8}$ of SSTL and RSL at a transfer rate of 1Gbit/s respectively.

4. Receiver

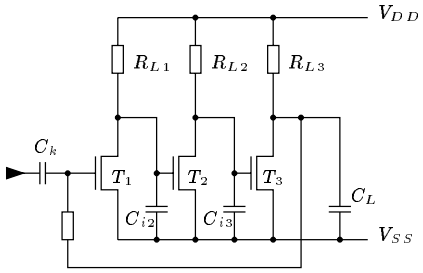

Figure 6. LNA input stage

A realized receiver circuit for the CCI-interface consists of a Low Noise Amplifier (LNA) which is designed to be able to sense mV-signals and a static Flipflop. The input stage of the LNA consists of three cascaded common-source amplifiers (Fig. 6). A high ohmic feedback resistor between the receiver's input and the output is used for self-biasing and to keep T1-T3 in saturation. The stability of the feedback loop is guaranteed for all values of the feedback resistor as long as the pole of the open-loop amplifier

$$p_3 = \frac{g_{L3} + g_{03}}{C_L} \tag{1}$$

is the dominant one whereby g_{L3} and g_{03} is the conductance of R_{L3} and T_3 respectively. The whole receiver circuit is shown in Fig. 7. It consists of one additional cascaded common-source amplifier and a NMOST and a PMOST one. The last ones generate a SET and a RESET signal for the Flipflop. The output voltage is the regenerated NRZ-signal. With no input signal the output of the NMOST apmlifier is a HIGH signal and the PMOST's ouput is a LOW one. The Flipflop does not change it's state.

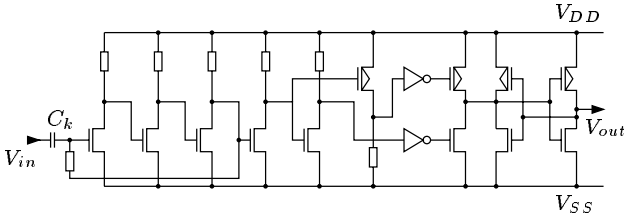

Figure 7. LNA receiver circuit

5. Measurements

The receiver is built in a 0.35μm technology. The coupling capacitance is realized as a Poly1-Poly2-capacitance. For the feedback a long channel NMOST in parallel with a PMOST is used as resistor. The load resistor is realized as a poly resistor with high ohmic poly material. Fig. 8 shows the die photo. The eye pattern is measuered at 1Gb/s at a supply voltage of 1.5V (Fig. 9). The height of the eye does not reach 1.5V because of the termination resistors in the measuring circuit. The measured current dissipation of the LNA-receiver is 1.1mA.

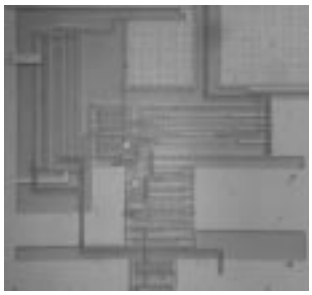

Figure 8. Die photo

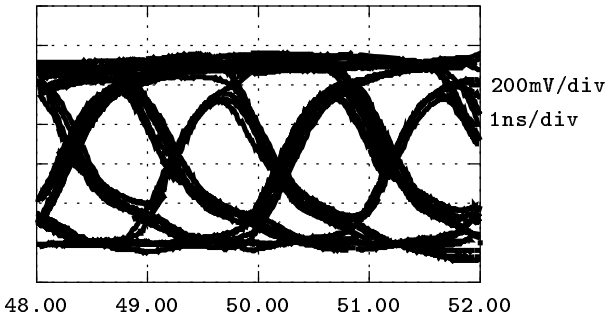

Figure 9. Eye pattern of the receiver at 1Gb/s

A bus with five I/Os has been built and analyzed. The measured outputs of the first and the fourth memory module are shown in Fig. 10 for two different NRZ-signals at a data rate of 300Mb/s.

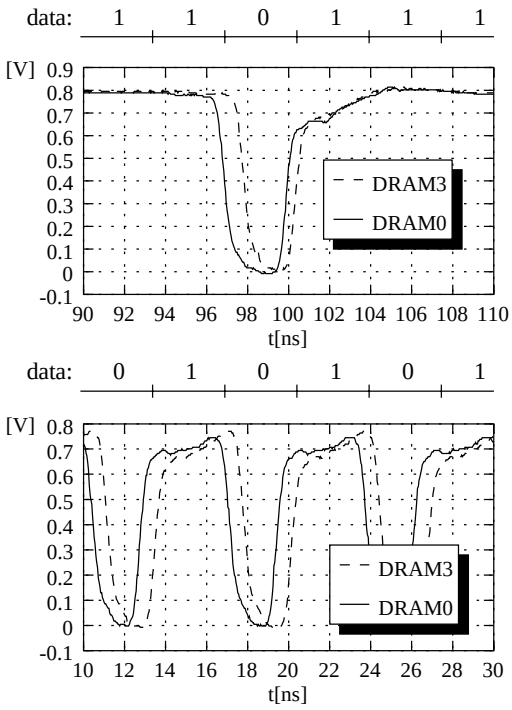

Figure 10. Measured output of DRAM0, DRAM3 (Fig. 2) at 300Mb/s

6. Conclusion

This work proposes a new interface for bidirectional multipoint connections like Controller-DRAM-busses. The capacitive coupling interface offers both a high data transfer rate and low power consumption for the driver which is reduced to $\frac{1}{8}$ and $\frac{1}{4}$ compared to RSL and SSTL at 1Gb/s respectively. A self-biasing LNA receiver built in a 0.35μm-technology requires 1.65mW DC-power for working up to 1Gb/s.

Acknowledgements

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References

[1] G. P. Singh, R. B. Salems, “A 1.9V I/O Buffer with Gate-Oxide Protection and Dynamic Bus Termination for 400 MHz UltraSparc Microprocessor”, *International Solid-State Circuits Conference*, IEEE, 1999, pp. 274-275.

[2] B. Lau, Y. -F. Chan, “A 2.6GByte/s Multipurpose Chip-to-Chip Interface”, *J. Solid-State Circuits*, IEEE, 1998, pp. 1617-1625.

[3] Y. Morooka, “Source Synchronization and Timing Vernier Techniques for 1.2GB/s SLDRAM Interface”, *International Solid-State Circuits Conference*, IEEE, 1998, pp. 160-161.