9.4 A 10Gb/s SONET-Compliant CMOS Transceiver with Low Cross-Talk and Intrinsic Jitter

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A single-chip full-rate 4:1 serializer/deserializer consuming less than 1W in a standard 0.13µm CMOS technology is presented. Previous full-rate designs are most commonly known in SiGe and BICMOS technologies, e.g. [1]. A special power supply concept is devised to suppress cross-talk between receiver and transmitter. This in conjunction with a high-Q notchched inductor layout in the VCO yields a phase jitter that is five times below the SONET specifications. Due to the full-rate architecture, the CDR can be used as a stand-alone IC without any need for demultiplexing as opposed to half-rate architectures [2]. The transceiver locks automatically to all data rates in the range of 9.95 to 10.7Gb/s making it suitable for most 10Gb applications.

The TX consists of a CMU and a 4:1 MUX, while the RX comprises a limiting amplifier (LIA) followed by a CDR and a 1:4 DEMUX. No additional external components are required. All high-speed circuitry is realized in differential current mode logic [3] employing synthetic inductor loads to increase bandwidth and per sub-block linearly regulated supplies, which allows maximum signal swing without exceeding device breakdown voltages. RX/TX cross-talk is minimized by, firstly, local capacitive coupling of the regulated supplies to a common ground plane, and secondly, by providing a very low impedance path with as many bond wires as possible to external ground. As the supply regulators provide isolation of the local supplies from the global one it is ensured that there is only one low impedance path from every supply node to external ground. Thus any undamped LC loops prone to peaking are avoided. Furthermore, no external decoupling capacitances that could prove to be inductive at high frequencies, are needed.

All VCOs share a basic building block and operate at 10GHz. It consists of a cross-coupled NMOs differential pair providing the necessary negative transconductance, a single loop inductance, a pn-junction varactor and an array of metal-insulator-metal (mim-) capacitors. The inductor is notched (see Fig. 9.4.1), which greatly reduces skin and proximity effects. Measurements confirmed an increase in inductance by 6% and in quality factor by 30% to a value of 26 at 10GHz. The pn-varactors with a tuning range of 300MHz are used for continuous tuning during normal operation of the PLL. The mim-capacitors are used to initially calibrate the VCO to a reference clock achieving an accuracy of 1% within a range of 1.2GHz. Thus, a wide tuning range and an excellent phase noise can be accomplished, which is essential for CMU performance.

The CMU VCO achieves a phase noise of -118dBc at 1MHz drawing 6.5mA from a 1.2V supply. Its figure of merit [4] is 190. An optimum flat jitter transfer function of the CMU is obtained by keeping PLL loop bandwidth constant. This is accomplished by adjusting the charge-pump current to compensate the non-linear VCO gain characteristics. The full-rate design allows to decrease incoming data jitter as the 4:1 MUX is retiming the output data at full 10GHz. The eye-diagram, measured with a 2^31-1 PRBS input pattern, is shown in Fig. 9.4.2. The phase noise spectrum of the TX clock can be seen in Fig. 9.4.3. Integration according to SONET OC-192 yields a jitter (rms) of 200fs, which is five times below the maximum allowed (1ps).

The LIA in front of the CDR provides 20mV input sensitivity at a bandwidth of 7GHz. Its topology is similar to that presented in [5], yet, five gain stages with synthetic PMOS inductor loads are used in addition to the common-gate input stage. Inductive peaking is not used to its full extent as it causes horizontal closure of the eye pattern due to increased group delay distortion. The bandwidth of the offset cancellation loop is set to 50kHz to keep baseline wander low.

The CDR VCO consists of two cross-coupled VCO building blocks forming a quadrature oscillator. The existing pn-varactors are part of a frequency tuning loop, while four pn-varactors are added to form a fully differential bang-bang [6] phase loop (see Fig. 9.4.4). In the CDR an extremely fast phase response together with maximum suppression of VCO jitter is achieved by the combination of a bang-bang architecture and a quadrature VCO. Additionally the fully differential phase loop and the pseudo-differential frequency loop offer superior power supply rejection.

For long runs of consecutive 0’s and 1’s the bang-bang architecture has the drawback of phase drift and additional jitter. To overcome this issue, the charge-pump is deactivated and the bang-bang control voltage is set to zero when a counter detects a long run. An intrinsic jitter of less than 10ps (peak-to-peak) is measured for a 2^31-1 PRBS pattern. The fully SONET/SDH compliant input-jitter-tolerance is shown in Fig. 9.4.5. The recovered 10-Gb/s data is fed to a 1:4 DEMUX consisting of 1:2 DEMUX cells in a binary-tree structure.

A micrograph of the chip, as fabricated in 0.13µm CMOS process, is shown in Fig. 9.4.7. The transceiver operates from 9.95Gb/s to 10.7Gb/s with a BER below 10^-12. The receiver input sensitivity is 20mV. The transmitter clock has a jitter of 200fs (rms) and 2ps (pp), while the recovered clock has a jitter of 1.1ps (rms) and 8.3ps (pp). Cross-talk measurements with 20ppm RX/TX reference-clock offset reveal a low additional jitter of 100fs (pp) on the 10GHz transmit clock, which confirms the presented power supply approach. The transceiver performance is summarized in Fig. 9.4.6.

Acknowledgments:
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References:
Technology: CMOS 0.13um, 1-poly 8-metal
Supply voltage: 1.2V / 2.5V
Power Dissipation (with LIA): 980mW (<1.2W)
Chip size: 3mm x 5mm
Bit rate: 9.953/10.31/10.664/10.709Gb/s
Input data sensitivity: 20mVpp single-ended applied
Recovered clock jitter (Inp. 2.5GHz Sinew.): 0.4ps (rms) in 50KHz-80MHz
Recovered clock jitter (Inp. 2^31-1 PRBS): 1.1ps (rms), 8.3ps (pp) full bandwidth
Jitter tolerance: >0.45 UIpp
Receiver jitter transfer peaking: < 0.1dB
Transmitter jitter bandwidth: 5 MHz
Transmitted clock jitter: 5ps (pp) and 740fs (rms) full bandwidth
Transmitted CLK jitter: 0ppm RX/TX offset: 2ps (pp) and 200fs (rms) in 50KHz-80MHz
Transmitted CLK jitter: >20ppm RX/TX offset: 1.1ps (pp) and 220fs (rms) in 50KHz-80MHz
Transmitter jitter transfer peaking: < 0.1dB
Transmitted serial data swing: 800mV
differential peak-to-peak
VCO capture range (coarse-tuning): 1.2 GHz nom. freq. 10.31GHz
VCO locking range (fine-tuning): 300 MHz nom. freq. 10.31GHz
Figure 9.4.7: Chip micrograph of the 10Gb/s CMOS transceiver.
Figure 9.4.1: Transmitter block diagram with CMU, LC VCO and MUX.
Figure 9.4.2: 10GHz CMU clock and eye diagram of $2^{31}-1$ PRBS output data.
Figure 9.4.3: Phase-noise measurement of the CMU-PLL.
Figure 9.4.4: Full-rate four-phases CDR with quadrature LC-VCO.
Figure 9.4.5: Input jitter tolerance measurement of the receiver.
### OC-192 Transceiver Performance Summary

<table>
<thead>
<tr>
<th>Specification</th>
<th>Specification Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>CMOS 0.13um, 1-poly 8-metal</td>
</tr>
<tr>
<td>Supply voltage</td>
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<tr>
<td>Power Dissipation (with LIA)</td>
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<td>Chip size</td>
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<tr>
<td>Bit rate</td>
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</tr>
<tr>
<td>Input data sensitivity</td>
<td>20mVpp single-ended applied</td>
</tr>
<tr>
<td>Recovered clock jitter (Inp. 2.5GHz Sinew.)</td>
<td>0.4ps(rms) in 50KHz-80MHz</td>
</tr>
<tr>
<td>Recovered clock jitter (Inp. $2^{31}-1$ PRBS)</td>
<td>1.1ps(rms), 8.3ps (pp) full bandwidth</td>
</tr>
<tr>
<td>Jitter tolerance</td>
<td>&gt;0.45 Ulpp</td>
</tr>
<tr>
<td>Receiver jitter transfer peaking</td>
<td>&lt; 0.1dB</td>
</tr>
<tr>
<td>Transmitter jitter bandwidth</td>
<td>5 MHz</td>
</tr>
<tr>
<td>Transmitted clock jitter</td>
<td>5ps(pp) and 740fs(rms) full bandwidth</td>
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<td>Transmitted CLK jitter 0ppm RX/TX offset</td>
<td>2ps(pp) and 200fs (rms) in 50KHz-80MHz</td>
</tr>
<tr>
<td>Transmitted CLK jitter ±20ppm RX/TX offset</td>
<td>2.1ps(pp) and 220fs (rms) in 50KHz-80MHz</td>
</tr>
<tr>
<td>Transmitter jitter transfer peaking</td>
<td>&lt; 0.1dB</td>
</tr>
<tr>
<td>Transmitted serial data swing</td>
<td>800mV differential peak-to-peak</td>
</tr>
<tr>
<td>VCO capture range (coarse-tuning)</td>
<td>1.2 GHz nom. freq. 10.31GHz</td>
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Figure 9.4.6: OC-192 Transceiver performance summary.
Figure 9.4.7: Chip micrograph of the 10Gb/s CMOS transceiver.