A Varactor with High Capacitance Tuning Range in Standard 0.25µm CMOS Technology

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Abstract

This paper presents a novel MOS varactor with outstanding capacitance tuning capabilities. Several test structures have been fabricated in standard digital 0.25µm CMOS technology. The novel varactor features a $C_{\text{max}}/C_{\text{min}}$ ratio of 5.3:1. Quality factors range from 16 to 190 with an average $Q$ of 86 at 2GHz. Thus it is outperforming all standard CMOS varactors reported up to now.

1. Introduction

LC-Tank Voltage Controlled Oscillators (VCOs) are widely used in Radio-Frequency Circuits. The core of these circuits is comprised of an integrated inductor and an integrated voltage controlled capacitance, called varactor. The values of the constant inductance $L$ and variable capacitance $C$ determine the frequency at which the VCO oscillates. To cover a large frequency band it is necessary to use a varactor with large tuning range $C_{\text{max}}/C_{\text{min}}$. For low phase noise of the VCO the passive elements of the tank are required to have large quality factors.

MOS-Varactors have proven to be superior to PN-Diode-Varactors [1],[3] in terms of power consumption, phase noise and tuning range. A variety of MOS-Varactors have been reported reaching capacitance ratios of up to 3.3:1 [2].

This work presents a novel varactor featuring a $C_{\text{max}}/C_{\text{min}}$ ratio of 5.3:1. It was fabricated in a standard 0.25um digital CMOS process with Shallow Trench Isolation (STI).

2. Device Structure

Figure 1 shows a cross-sectional view of the novel device.

![Cross-section of novel device](image)

Figure 1. Cross-section of novel device

It is similar to an accumulation mode varactor (A-MOS) [3]. However, in the new
structure, the well contacts (equivalent to source/drain contacts in an A-MOS varactor) are separated from the active area by STIs to reduce parasitic capacitances. The manufacturing process requires that the poly gate overlaps the STIs to a certain amount. Reducing the overlap improves the properties of the proposed structure.

The variable capacitance is the capacitance between gate and all the other terminals of the varactor. It is tuned by the N-well voltage $V_w$, while the RF-signal is applied to the gate in addition to the DC voltage $V_g$.

### 3. Device Characteristics

Due to the close similarity of the structures, the tuning behaviour of the new structure is close to that of an A-MOS varactor, as well described in [3].

Figure 2 shows the lumped elements that appear in the novel varactor at depletion.

![Figure 2. Lumped elements in the new structure at depletion. Dashed lines indicate depleted regions](image)

$C_{ox}$ is the gate oxide capacitance, while $C_d$ is the variable depletion capacitance in series. $C_o$ are overlap and $C_f$ fringing capacitances. $C_f$ and $C_o$ can be considered to be constant and are always parallel to $C_{ox}$ and $C_d$. $R_g$ denotes the series resistance introduced through the poly gate. $R_{w1}$ to $R_{w4}$ describe the resistive path from gate to N-well contacts (resistances within the highly doped N-well contacts are negligible.)

As $C_o$ is small, simple formulas can be found for the effective $R$ and $C$:

$$R = R_g + R_{w1} + \frac{1}{2} (R_{w2} + R_{w3} + R_{w4})$$  \[Eq.1\]

$$C = (C_{ox}^{-1} + C_d^{-1})^{-1} + 2 (C_f + C_o)$$  \[Eq. 2\]

Both values, $C$ as well as $R$, depend strongly on the applied voltages. The situation at zero N-well voltage $V_w$ is as follows: at low gate voltages $V_g$, the varactor is in depletion. $C_d$ is at its minimum which results in a small overall capacitance $C$. With increasing $V_g$ the device is moved into accumulation, $C_d$ vanishes and we see a large capacitance given by $C_{ox}$ and the parallel parasitics.

The major voltage dependence of $R$ stems from $R_{w1}$, as it describes the resistance from the border of the depletion region beneath the gate to the region below the STIs. Decreasing $V_g$ leads to a larger depletion region with smaller $R_{w1}$ and $R$. The resistances $R_g$ and $R_{w2}$ to $R_{w4}$ are independent of $V_g$.

Increasing $V_w$ increases the gate voltage at which accumulation occurs. The basic $V_g$ dependent behaviour of $C$ and $R$ does not change, it is only shifted towards higher $V_g$ by the amount $V_w$ has been increased.

The weak dependence of $R$ on $V_w$, due to the increasing depletion region between well and substrate, is negligible.

As $C$ and also $R$ increase with increasing $V_g$ the quality factor $Q$ decreases strongly with increasing $V_g$, since $C$ and $R$ determine $Q$ by

$$Q = (2\pi f R C)^{-1}$$  \[Eq. 3\]
4. Improved Tuning Range

[Eq.2] shows that there are two ways to improve tuning range: a reduction of parasitic capacitances and/or a decrease of the minimum possible $C_d$. The influence of both possibilities is tested with the proposed structure.

The constant parasitic capacitances inhibit large ratios $C_{\text{max}}/C_{\text{min}}$ when using MOSFET–varactors [3]. Figure 3 depicts the relevant capacitances of an A-MOS varactor in depletion.

The new structure reduces overlap and fringing capacitances in comparison to conventional MOSFET–varactors (compare Figures 2 and 3). The overlap capacitances are smaller since the STI is much thicker than the gate oxide. The reduction of fringing capacitances is simply achieved by increasing the distance of the gate to the N-well contacts in comparison to the distance of the gate to source and drain regions in MOSFETs. By proper layout the parasitic capacitances can easily be made much smaller than the ones appearing in conventional MOSFETs.

Decreasing the minimum $C_d$ is achieved by implementing a small grounded p+ region at each finger according to [4]. This allows the device to reach deep depletion.

5. Measurement Results

Several prototypes of the proposed varactor have been fabricated in multifinger layout to reduce series resistances. A die photograph is shown in figure 4.

Finger length varies from 8µm to 16µm and active area widths from 0.32µm to 0.64µm. The total active area of each device is 307.2µm². The width of the STIs and therefore the distance between poly gate and N-well contacts is the same in each case.

Two-Port S-Parameters with the gate and the well contacts as nodes have been measured using an HP8510.

Values for $C$ and $Q$ are retrieved by

\[
C = - (2\pi f \text{Im}(Y_{11}^{-1}))^{-1}
\]

\[
Q = - \text{Im}(Y_{11}^{-1}) / \text{Re}(Y_{11}^{-1})
\]

All evaluations are carried out at a frequency of 2GHz.

Measurement results show that using large active area width and large finger length is advantageous. Figure 5 presents capacitance curves at 2GHz for the device with active area width of 0.64µm and finger length of 16µm. It features a $C_{\text{max}}/C_{\text{min}}$ ratio of 5.3:1. In comparison active area width of 0.32µm and finger length of 8µm achieves a $C_{\text{max}}/C_{\text{min}}$ ratio of 3.8:1 only.

Figure 3. Lumped elements of an A-MOS varactor in depletion. Dashed lines indicate depletion regions.

Figure 4. Die photograph
Figure 5. Capacitance at 2GHz

Figure 6 shows the quality factor at 2GHz of the varactor with a $C_{\text{max}}/C_{\text{min}}$ ratio 5.3:1. It features a maximum $Q$ of 190, a minimum $Q$ of 16 and a $Q$ of 86 averaged over $V_w$ and $V_r$. The CMOS varactor with the largest reported tuning range of 3.3:1 featured a maximum $Q$ of 20 [2].

Figure 6. Quality factor at 2GHz

To investigate the influence of the p+ regions two identical devices, one with and one without p+ region, were fabricated (active area width: 0.32µm and finger length: 8µm). It was found that using the p+ regions increases the $C_{\text{max}}/C_{\text{min}}$ ratio. At 2GHz the varactor without p+ region achieved a capacitance ratio $C_{\text{max}}/C_{\text{min}}$ of 3.66, while adding the p+ region increases the value to 3.82.

6. Conclusion

A novel varactor structure is implemented in a standard digital 0.25µm CMOS technology with shallow trench isolation. Several test structures have been fabricated and measured. The novel varactor features an outstanding $C_{\text{max}}/C_{\text{min}}$ ratio of 5.3:1. At 2GHz quality factors range from 16 to 190 with an average $Q$ of 86.

7. References


The proposed structure is patent pending.