Degradation Modeling of Semiconductor Devices and Electrical Circuits

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Abstract

A mathematical description for the degradation of semiconductor devices and electrical circuits is presented. It is based on the assumption that the reason for degradation is a destruction of internal structures, caused by the input of energy. The formulation is tested with the Simulation of an IGBT module.

Additionally a method is presented to shorten the simulation time as much as possible.

1 Introduction

The reliability of semiconductor devices and electrical circuits is a very important topic for circuit designers and manufacturers. So far it is dificult to predict the lifetime of a device in a circuit, since its lifetime strongly depends on the Operation of it. One of the most significant Parameters is the temperature. For example the investigations of [7] have shown, how the lifetime of IGBT modules depends on the temperature Swing and the average temperature during power cycles.

The purpose of this work is to develop a degradation model which makes it possible to perform reliability simulations. This means, that with the help of circuit simulations it tan be estimated, how the lifetime of a device will be influenced by the kind of Operation and the occurring stress of the device.

2 Degradation-Model

2.1 Description of the Modeled Failure Mechanism

The first step of the model development is to detect the dominant failure mechanisms.

The reason for failure is in many cases a very slowly increasing degradation somewhere in the device or package. The energy which is dissipated during Operation tan Cause many different changes in a material, like hardness and form modifications, flowing movements etc. But finally a Crack-growth is mainly responsible for the failure of a device.

Regions concerned by Crack-growth are generally the contact surfaces of the junction between two materials. These areas are very inhomogeneous compared with the homogeneous materials used for semiconductors. The different thermal expansion coeffrcients of two materials lead to large tensions at the junction and finally to Crack growth.

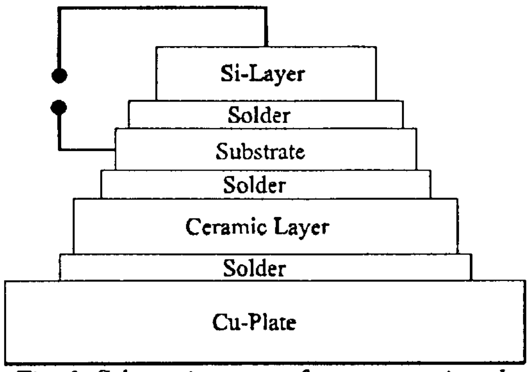

Fig. 1: Schematic set-up of a power semiconductor module.

In the case of the investigated IGBT modules two main failures could be observed: lift-off of bond wires and cracks of the solder contact between the silicon chip and the substrate of the package (Fig. 1).

The second effect is considered in the following. During operation the device heats up significantly due to energy losses mainly in the silicon layer. The heat flows through the different layers shown in Fig. 1 to the Cu-plate where a heat sink is attached.

The variations of temperature can lead to a damage of the layers or the contacts between layers. The damage increases with the ongoing temperature cycling which reduces the area accessible for the heat and/or current flow. This results in an increase of the electrical and thermal resistances and leads to a further rise of the temperature and finally to the destruction of the device.

2.2 Modelling Approach

An IGBT model for circuit simulation is applied for the description of the electrical and thermal behaviour of the device [6]. With the help of a thermal equivalent circuit that simulates self-heating, the degradation model can describe the increases of electrical and thermal resistances due to the decrease of the conducting area. The thermal equivalent circuit uses the thermal resistances R_{th} and the thermal capacitances C_{th} of the different layers (Fig. 2). These elements change their values with time according to the degradation of the material.

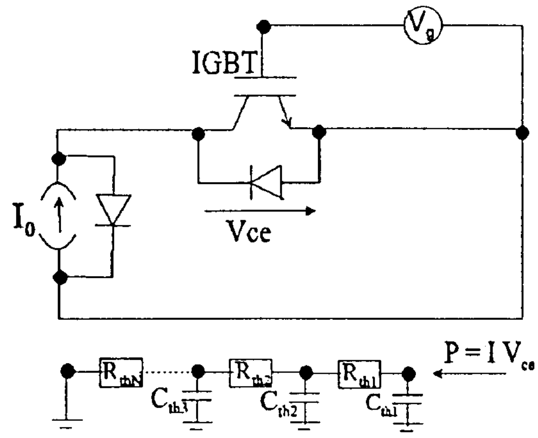

Fig. 2: The electrical and thermal circuit used in this work.

2.3 Basic Equations of the Degradation-Model

2.3.1 Energy Conservation

The energy rates entering and leaving a volume element are given by:

$$P_{el} + \dot{Q}_{in} = \dot{U} + \dot{Q}_{out}. \qquad (2.1)$$

The deposition of energy U in a volume element results in a temperature rise of that element (Fig. 3). Most of the energy is stored in the internal energy of that element, but a small part may be used to cause irreversible changes in its structure.

$$\dot{U} = \dot{U}_{th} + \dot{W} \qquad (2.2)$$

$\dot{W}$ may be the power used in the layer for any kind of irreversible work, like deformations

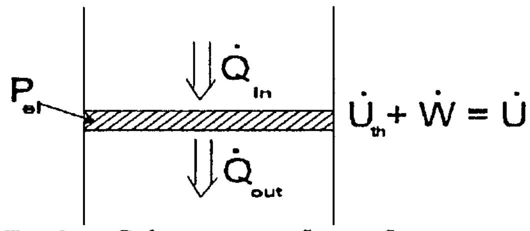

Fig. 3: Relevant energy flows influencing a layer.

and crack growth, $\dot{U}_{th}$ is the change in the internal (heat) energy and $\dot{U}$ is the sum of both. P_{el} is the electrical power-loss, $\dot{Q}_{in}$ is the in-coming heat from one adjacent layer and $\dot{Q}_{out}$ is the heat-flow to the other (Fig. 3).

The first assumption is that $\dot{W}$ is a changing percentage p of the total power $\dot{U}$ put into the layer:

$$\dot{W} = p\,|\dot{U}|. \tag{2.3}$$

This means that $\dot{W}$ is proportional to the temperature variation:

$$\dot{W} \propto |\dot{T}|. \tag{2.4}$$

2.3.2 Growth Velocity

The considered degradation mechanism is a crack growing with time. The velocity of crack growth $\dot{r}_c$ depends on temperature; this dependence is described with an expression according to the Arrhenius function:

$$\dot{r}_c = \dot{r}_{c0} e^{-\frac{E_{aw}}{kT}}. \tag{2.5}$$

Here E_{aw} is the activation energy for crack growth and $\dot{r}_{c0}$ is the crack growth velocity if no activation energy is necessary ([4] and [3]).

2.3.3 Relation between Energy and Crack Growth

The velocity of crack growth $\dot{r}_c$ is related to the power $\dot{W}$ causing irreversible changes of the material. It is assumed that this relation is not constant; the following expression has been obtained by empirical considerations:

$$\dot{W} = (\chi\dot{r}_c + (1-\chi)\dot{r}_{c0})\frac{W_{rest}}{\lambda} \tag{2.6}$$

with

$$W_{rest} = W_{tot} - \int_0^t \dot{W}dt. \tag{2.7}$$

χ is the percentage of irreversible changes which result in crack-growth. λ is a proportion factor with the dimension of length. W_{tot} is the total amount of energy necessary to destroy the layer-contact completely. It is assumed that W_{tot} has a fixed value for each type of device.

Setting $\dot{W}$ proportional to W_{rest} means that the energy required for crack growth decreases with increasing damage of the material. This results in an acceleration of the crack growth with time.

2.3.4 Growth Function

The combination of the equations above then leads to a formulation that describes the growth velocity of a crack radius r_c as a function of the input power and the temperature of the layer:

$$\dot{r}_c = \lambda \frac{\dot{W}}{W_{tot} - \int_{t_0}^{t} \dot{W}dt}\left[\chi + (1-\chi)e^{\frac{E_{aw}}{kT}}\right]^{-1}. \tag{2.8}$$

2.3.5 Electrical and Thermal Properties

The growth of the crack-radius r_c is equivalent with a decrease of the conducting area A. This leads to an increasing electrical (R_{el}) and thermal resistance (R_{th}),

$$R_{el} = \rho\frac{d}{A};\;\; R_{th} = \frac{d}{\lambda_{th}A}, \tag{2.9}$$

and to a decreasing thermal capacity

$$C_{th} = dA\rho c. \tag{2.10}$$

λ_{th} is the thermal conductivity, ρ the specific mass, c the specific thermal capacitance and d the thickness of the layer. Furthermore it is assumed for simplicity that the area A is the same for the thermal and electrical values.

3 Shortening of the Simulation Cycles

To simulate the degradation of a device, it might be necessary to go through some ten- or hundred-thousands of cycles. To avoid this, it is possible to skip every z cycles. If z<<N (where N is the total amount of cycles until destruction) the Change of bc and the Change in the lost energy AW during the skipped z-Periods might be negligible. With

$$p=\frac{N}{z}, \tag{3.11}$$

and when bc is not significantly changed during z periods, one receives

$$\Delta r_c \cong \sum_{n=1}^{N^*} z\lambda \frac{\Delta W_n}{W_{tot}-\sum_{m=1}^{n} z\Delta W_m}\left[\chi+(1-\chi)e^{\frac{E_{aw}}{kT_n}}\right]^{-1} . \tag{3.12}$$

4 Resul ts

The degradation model has been implemented in the circuit Simulator Saber.

As example of the obtained results, the degradation of IGBT-modules used in the circuit shown in Fig. 2 is presented. For this circuit results of experiments have been available which could be used to determine the required model Parameters and to compare the simulations with measurements. The IGBT modules are periodically operated with constant current for a certain period of time. The power loss in the device causes a temperature rise which has been measured.

The results of these experiments are shown in Fig. 4. This figure Shows the amount of power-cycles until destruction, as a function of the temperature shift *AT.* It Shows three series of experiments which differ in the medium temperature range.

The corresponding simulations have been performed with an IGBT model presented in [6]. The Simulation results in *Fig. 5* show the increase of the IGBT on-state voltage caused by the increase of the ohmic resistance due to the degradation of the conducting layer. Three different temperature Swings resulting fiom different levels of the load current are applied. The figure Shows afier how many switching cycles the destruction of the device is initiated by a dramatic rise of the ohmic and thermal resistances. These cycle numbers arc also inserted in Fig. 4 . Good agreement with the measured results tan be Seen.

The model tan now be used to simulate degradation under realistic conditions and to predict the lifetime when the Operation of the devices in a circuit is not as regular as in the example above but varies in a very wide range.

5 Conclusion

A formalism to calculate the degradation of semiconductor devices and electrical circuits has been developed. It is based on the assumption that tensions caused by temperature gradients within the device Cause a Change of the device morphology and a Crack-growth that leads to the final failure of the device.

The degradation model offers the new design capability of reliability Simulation and optimisation. It tan be analysed, which conditions of Operation are necessary to guarantee a certain lifetime of the devices used in a circuit.

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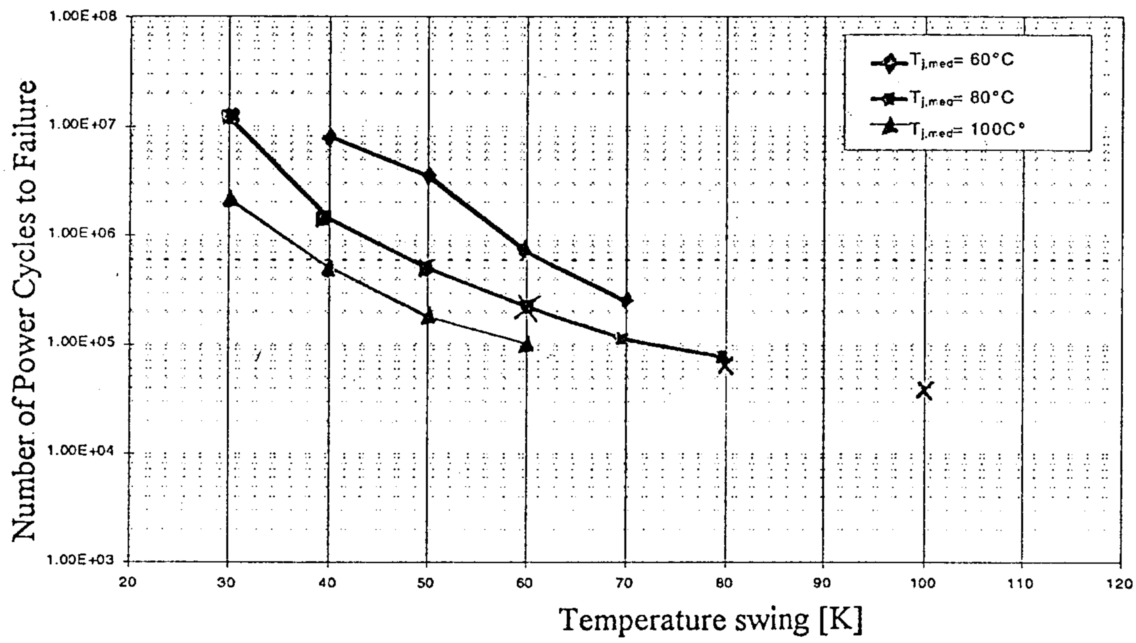

Fig. 4: Maximum Number of Power-cycles – Dependence on junction temperature swing and absolute temperature with $T_{j,med}=(T_{j,max}+T_{j,min})/2$ (measured data from [7]). ♦, ■, ▲ measurements, × simulations.

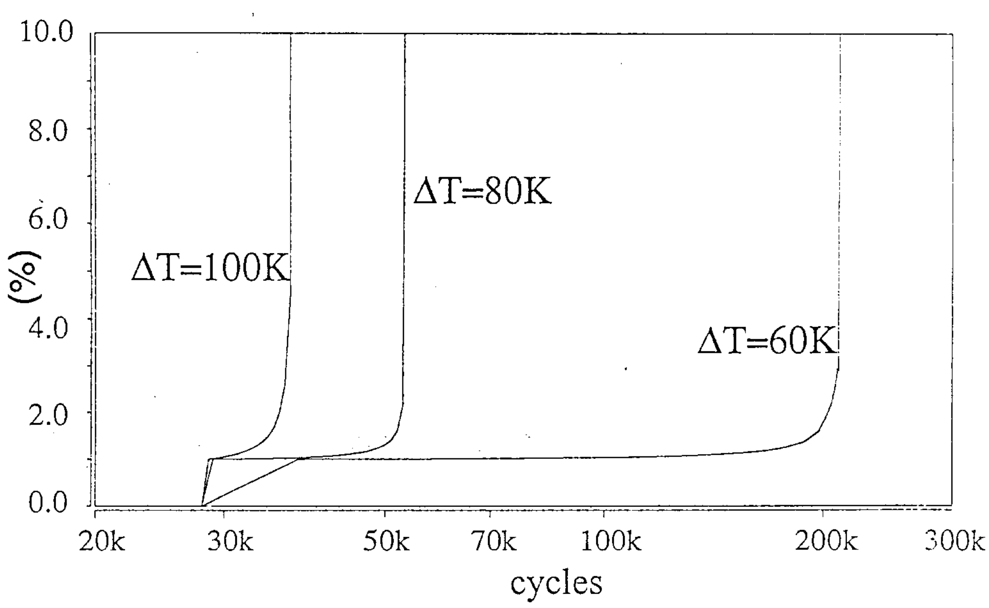

Fig. 5: Relative change in the cathode-emitter voltage V_{ce}/V_{ce0} as a function of power cycles. Destruction is defined as the point where the change has reached 10%.