Status and Trends of Power Semiconductor Device Models for Circuit Simulation

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***Abstract*—The current status of research in the field of power semiconductor device models is reviewed. For this purpose, the basic modeling problems and research issues, which have to be overcome in this field, are discussed. Recently, some new and quite promising modeling concepts have been proposed, which are compared with more traditional ways of achieving an efficient tradeoff between the necessary accuracy, required simulation speed, and feasibility of parameter determination. From this comparison, a prediction of the future evolution of circuit simulation models for power semiconductor devices naturally emerges. Many of the different concepts are expected to survive only in an application niche, where their specific points of strength are important. However, three modeling concepts have already been proven to be successfully applicable to the complete spectrum of power semiconductor devices and have their strength for different grades of complexity of the power circuit. A revolutionary development from anticipated or longdue breakthroughs is on the other hand not expected in the foreseeable future.**

***Index Terms*— CAD, circuit simulation, modeling, parameter extraction, power semiconductor devices.**

I. INTRODUCTION

IN RECENT years, research on power semiconductor device models for circuit simulation has intensified. Several research groups throughout the world have tried to advance the state of the art with respect to the status summarized in previous review articles [1], [2]. A number of new concepts for trimming the basic physical equations to the requirements of a power semiconductor device model for circuit simulation have been proposed [42], [43], [53], [69], [75], [101], [117], [119], [122], [129], [134], [140]. The special challenge in developing such models for circuit simulation results from the need to simultaneously fulfill contradicting requirements like high quantitative accuracy, low demand of computation power, and physical and easy accessible model parameters. At least a favorable tradeoff between these contradicting requirements is necessary.

Responsible for the above development are the general economical boundary conditions, which also demand an improved efficiency and reliability in the design and realization of power electronic circuits. Such an improvement can only be achieved through an upgrading of the computer-aided design (CAD) methodology and their application from the beginning of the development phase of a power electronic circuit. A key element for achieving such an upgrade in CAD methodology is the availability of high-quality power device models for circuit simulation.

Traditionally, the design tools for power circuits have employed very simple power semiconductor models, which only featured a digital switching (abrupt or linear) behavior as well as a fixed resistance in the conducting state. This standard is far below the state of the art in the design of integrated circuits and was acceptable in the past because power circuits used to be operated at small switching frequencies. Therefore, the detailed switching characteristics of the active power semiconductor devices were of second-order importance, and the tradeoffs in the power circuit design were dominated to a large extent by capacitances and inductances. The situation has changed as applications tend to move to power circuits operated at higher switching frequencies. From this trend, the opportunities of reduced power losses and reduced sizes for the complete power system result. Moreover, international competition is forcing companies to speed up introduction of new products in the different applications fields of power electronic circuits without sacrificing product quality and reliability. The best way to take advantage of those opportunities to increase product innovation, reduce prototyping, and cope with economical pressure is, of course, to employ a CAD methodology, which accurately predicts the functionality and reliability of a specific power circuit design. This again means that high-quality power semiconductor device models for circuit simulation are required.

The trends and requirements for an upgrade of the CAD methodology for power circuit design as well as the necessity of improved power semiconductor device models for circuit simulation have not only been recognized on the academic side, but by the software industry too. A few specialized software vendors (like Analogy, Anacad, Mentor, Meta-Software, MicroSim, and Intusoft) have already reacted to these market opportunities and are offering enhanced support for the design of power electronic circuits. This includes also improved power device models incorporating many of the recent advances of the ongoing research. In fact, the software vendors are participating to some extent in these research activities on power device models for circuit simulation and pushing them ahead. In this paper, we will not discuss in detail the different models, which each of the vendors is offering, but restrict ourselves to the basic problems of modeling power semiconductor devices for circuit simulation and the status of

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TABLE I

RELEVANCE OF BASIC PHYSICAL PHENOMENA FOR DIFFERENT POWER DEVICES (++ VERY IMPORTANT, + IMPORTANT, 0 TO BE INCLUDED, - LESS IMPORTANT, - - NOT APPLICABLE)

	Diode	BJT	Thyristor/GTO	MOSFET	IGBT, MCT
Resistivity Modulation	++	++	++	++	++
Charge Storage	++	++	++	-	++
MOS-Capacitances	- -	- -	- -	++	++
Electro-Thermal	+	+	+	+	+
Breakdown	o	o	+	o	o

the research efforts for overcoming these problems. However, the reader can be sure that software companies are eager to incorporate these research advances into their products and that he will be able to get CAD support for his practical design problems, which reflects the current state of the art.

In the following sections, we will first (Section II) give an overview of the basic problems, which have to be overcome in the development phase of a useful circuit simulation model for a power semiconductor device. We will then (Section III) concentrate on the various attempts and ideas applied in the past to solve these basic problems and group them into categories of similar modeling concepts. Emphasis is put on the new concepts, introduced in recent years, which helped to advance the state of the art significantly. The subject of the subsequent section (Section IV) is the issue of parameter definition and determination, which emerges as one of the crucial remaining challenges for achieving a wide acceptance and application of the intended upgrade in the CAD methodology for the design of power electronic circuits. On the basis of the material presented and discussed, we then try (Section V) to give a comparison and relative evaluation of the known modeling concepts and finally (Section VI) discuss especially the possible trends of further future development and improvement of the present state of the art. It is of course unavoidable that these last two sections will reflect to some extent personal views and opinions of the authors.

II. BASIC PHYSICAL PHENOMENA AND MODELING PROBLEMS

For the development of power semiconductor device models, several effects have to be considered with high priority since they dominate the static and dynamic device characteristics. These effects are not described correctly by standard device models (or they are not included at all) because their influence on low-power devices is less important or neglectable. An accurate description, however, is essential for power devices.

Table I gives an overview of the main effects and their importance for the different power devices.

Modeling of these effects is based on one-dimensional (1-D) calculations in most cases. The majority of power semiconductor devices, however, have a structure with distinct two-dimensional (2-D) or three-dimensional (3-D) features, and, therefore, the 1-D idealization can be insufficient to describe the effects accurately. But more dimensional calculations increase the difficulty and complexity of finding solutions by such a drastic amount that they are applied only exceptionally.

A. Resistivity Modulation

To sustain high blocking voltages, power semiconductor devices have a thick lightly doped semiconductor layer. The resistance of this region determines the voltage drop and power loss when the device is in its conduction mode. This resistance is variable and its dependence on voltage or current can be highly nonlinear. In unipolar devices (MOSFET), the variations are caused by variations of the effective current-conducting area and by the mobility degradation with an increasing electric field. In bipolar devices [diode, bipolar junction transistor (BJT), thyristor, gate turn-off thyristor (GTO), insulated gate bipolar transistor (IGBT), and MOS-controlled thyristor (MCT)], the low-doped layer is swamped by electrons and holes when the device is in its on state. The density of the injected charge carriers can be much higher than the level of the doping concentration, and the resistivity of the region is significantly reduced.

The resistance of a region with the boundaries x_1 and x_r and the area A is given by

$$R = \int_{x_l}^{x_r} \frac{dx}{qA(\mu_n n + \mu_p p)} \tag{1}$$

where n and p are the densities of electrons and holes, respectively, and μ_n and μ_p are the mobilities of the charge carriers. In most cases, the charge carriers are not distributed homogeneously, and their density depends on position, and in some cases, the mobilities also cannot be regarded as constants. During transient operation, the variation of the resistivity does not follow the changing current instantaneously—this effect can influence the switching behavior (e.g., forward recovery of power diodes), and in order to take it into account, a dynamic description of the charge distribution is necessary. Even if a solution of the time-dependent charge densities is found, the calculation of the resistance remains difficult since the integration in (1) is not possible without simplifications.

B. Charge Storage

The charge carriers, which are stored in the lightly doped region of bipolar devices during the conduction mode, must be extracted before the device can reach its blocking state. This effect causes switching delays and switching energy losses. Standard device models for circuit simulation use a quasi-static description of the charge carriers. It means that the charge distribution is always a function of the instantaneous voltages at the device terminals. This method is completely insufficient for power devices. A real dynamic description derived from the basic physical equations is required instead.

The charge stored in a low-doped region of a power device varies, under transient operation, with both time and position. This variation is determined by the ambipolar diffusion equation

$$\frac{dp}{dt} = -\frac{p}{\tau} + D\frac{d^2p}{dx^2} \tag{2}$$

where $p(x,t)$ is the density of the charge carriers, τ is the charge carrier lifetime, and D is the diffusion coefficient. This equation is valid in the case of high-level injection when hole and electron densities are approximately equal.

The slope of the charge carrier distribution is related to the currents—this relation is described by the transport equation

$$I = \left(1 + \frac{\mu_p}{\mu_n}\right)\left(I_n - qAD\frac{dp}{dx}\right) \tag{3}$$

where I_n is the electron current and I is the total current, the sum of electron and hole current. The integral of (2) together with the condition of (3) yields the charge control equation

$$\frac{dQ}{dt} = -\frac{Q}{\tau} + I_n(x_r) - I_n(x_l) \tag{4}$$

where x_r and x_l are the boundaries of the considered region and Q is the charge in this region.

One current component at each border is determined by the neighboring region. The total current is then obtained with (3), but this requires a solution of (2). Unfortunately, an exact analytical solution is not possible in the general case.

C. MOS Capacitances

Devices with isolated gate (MOSFET, IGBT, and MCT) have large capacitances which vary strongly with voltage in the different regions of operation. The capacitance of greatest importance is that between anode and gate. These are normally the output and input terminals of the device, and the resulting feedback has a dominating influence on the switching behavior. The capacitor is formed by the metal–oxide–semiconductor (MOS) structure resulting from the isolation of the gate from the semiconductor region. The value of the gate-anode capacitance C_{GA} can be calculated from the gate charge Q_G

$$C_{\mathrm{GA}} = \frac{dQ_G}{dV_{\mathrm{GA}}} = C_{\mathrm{ox}}\frac{dV_{\mathrm{ox}}}{dV_{\mathrm{GA}}} \tag{5}$$

where C_{ox} is the capacitance of the plate capacitor which is determined by oxide thickness and area of the structure. The voltage V_{ox} across the oxide is a highly nonlinear function of the gate-anode voltage V_{GA} since at the surface of the semiconductor, below the gate, different states of the charge are possible. These states are called accumulation, depletion and inversion. Depending on the state, the derivative in (5) can vary between one and zero. Solutions of (5) are usually obtained with approximations treating the states separately, but this can lead to problems of abrupt changes in the capacitance or its derivative at transitions between different regimes of operation. Furthermore, dynamic transition states are possible.

D. Electrothermal Interaction

Due to high energy losses, power devices can heat up significantly during operation. The device characteristics depend strongly on the device temperature, therefore, the changing temperature influences the device behavior. To consider this interaction between thermal and electrical characteristics, electrothermal device models are required.

The device temperature T is calculated with the equation of heat transport

$$\frac{dT}{dt} = \frac{\lambda}{C'_{\mathrm{th}}}\frac{d^2T}{dx^2} + \frac{P'}{C'_{\mathrm{th}}} \tag{6}$$

where C'_{th} is the thermal capacitance per volume, λ is the thermal conductivity of the material, and P' is the generated thermal energy per volume. Thermal models usually use an average device temperature, which is then applied to the temperature-dependent parameters of the model equations. The temperature, however, is distributed inside the device and high temperature peaks can be localized in small regions.

E. Breakdown

Breakdown in power semiconductor devices occurs not only in the case of failure; in many applications breakdown happens during regular operation of the device (e.g., at turn off of GTO's). The most common breakdown mechanism is the avalanche effect due to impact ionization, but Zener breakdown and punchthrough are also possible.

The current increase due to the generation of charge carriers by impact ionization can be expressed by a multiplication factor M_p

$$I_p(w) = M_pI_p(0) = \frac{I_p(0)}{1 - \int \alpha_p \exp \int (\alpha_n - \alpha_p)\, dx'\, dx} \tag{7}$$

where α_n and α_p are ionization coefficients which depend on the electric field $E(x)$

$$\alpha_p = a_p\mathrm{exp}\left(-\frac{b_p}{E(x)}\right) \quad \alpha_n = a_n\mathrm{exp}\left(-\frac{b_n}{E(x)}\right).$$

The integral in (7) cannot be solved analytically since the electrical field is not constant. Furthermore, there is a feedback of the generated charge carriers on the electric field and during transient operation, the onset of the avalanche breakdown can be shifted significantly by the current flowing through the high-field region (dynamic avalanche). Usually, however, a constant breakdown voltage is used to model breakdown.

III. MODELING CONCEPTS

To obtain models for the purpose of circuit simulations, relatively compact descriptions of the relevant effects must be

TABLE II
MODELING OF BASIC PHYSICAL PHENOMENA WITH DIFFERENT APPROACHES (+ APPLIED, 0 POSSIBLE, - NOT APPLICABLE)

	Functional Model	Approximate Solution	Transformation	Lumped Model	Numerical Solution
Resistivity Modulation	+	+	o	+	+
Charge Storage	+	+	+	+	+
MOS-Capacitances	+	+	-	+	o
Electro-Thermal	+	+	+	+	+
Breakdown	+	+	-	-	o

found because of practical restrictions in computing power. These descriptions must furthermore be implemented in the programs for circuit simulation.

The implementation occurs mainly in two ways: by so-called subcircuits or by mathematical functions. Mixed forms are also possible.

Subcircuit models are constructed by using conventional models which are available in the circuit simulation program and by combining them with passive components, switches, and controlled voltage and current sources. This method can lead to very complex and time-consuming models, and it is therefore mainly used if the simulation program does not provide the possibility to implement mathematical functions.

The much more efficient way is the insertion of model equations into the simulation program. However, this requires the respective capabilities to be available.

In most cases, it is not possible to obtain exact analytical solutions of the physical semiconductor equations, which are used as the basis [e.g., (1)–(7)]. Therefore, other methods must be used for the derivation of model equations. A large variety of approaches can be distinguished. Table II shows the most important methods and their applications to the different effects.

To explain the underlying ideas of the different approaches the example of charge storage is used. Modeling this effect can be regarded as the most challenging task in the construction of power semiconductor device models for circuit simulation.

A. Functional Model

The approach of a functional model treats the device as a "black box" and describes the externally observed behavior without a detailed consideration of the physical effects occurring inside the device [3]–[40].

1) Standard Low-Power Device Model: The standard low-power device models, which are available in circuit simulators, are adapted to power semiconductor devices by optimizing their parameters. Thereby, the parameters and model equations can lose their physical meaning, and a pure functional description may result. These models, however, are hardly able to simulate any high-voltage phenomena.

2) Lookup Table: In lookup tables, the data resulting directly from measurements or from calculations are stored and retrieved for simulation [18]. This method is well suited for DC characteristics, but it is much more difficult to use it for dynamic effects of the device in the environment of different circuits. The transient behavior of power semiconductor devices can depend on a large number of conditions which result from the state of the device before switching and the interactions of the device with other circuit elements during switching. Therefore, the effort becomes very large to consider all the situations caused by the varying conditions in many different circuit topologies.

3) Empirical Expressions: The equations of functional models are not obtained by rigorous derivations from the device physics. In many cases, they are selected arbitrary mathematical expressions which describe the externally observed behavior in a simplified way. But considerations of physical effects within the device can also be taken into account. If it is possible, the currents and voltages of the device terminals are approximated directly by straightforward functions. For a description of dynamic effects, however, it is often necessary to include additional variables into the equation set. These variables can be (but are not restricted to) internal variables of the device, e.g., the device charge. The relations between them and the external current and voltage waveforms are described by mathematical functions which are mainly obtained by intuitive assumptions. (These assumptions can be inspired by device physics, and, in some cases, they can be confirmed by theoretical derivations.) For example, the relation

$$Q(t) = -I(t)\tau_R \tag{8}$$

is used to approximate the reverse recovery of power diodes. τ_R is a time constant which determines how fast the turn-off reverse current of the diode decreases. A solution for the current is obtained with this relation and the simplified charge control equation (the difference of the electron currents is replaced by the total current). This solution, however, is valid only for the phase of turn off when the current decreases from its reverse peak to zero. Other switching phases must be described by other functions, and the solutions of the different phases must be adjusted to guarantee continuity.

B. Approximate Solution

The model equations of this approach are based on the device physics, but since exact solutions are not possible or restricted to a few special cases, appropriate mathematical representations are found to approximate the solution [41]–[115].

These approaches are purely empirical in many cases, but it is also possible to show that some functions come close to an exact solution under certain constraints of the boundary conditions.

1) Assumed Solution: The approximations applied to the time-dependent charge carrier distribution can be simple geometrical curves (e.g., straight lines and sine functions), which imitate the shape of the distribution [115]. The knowledge of how the shape must look like is obtained from theoretical considerations or numerical calculations (device simulators).

Some authors use different mathematical techniques to optimize the chosen functions and to obtain a close approximation to the diffusion equation and its boundary conditions. The solutions try in most cases to separate variables by a product assumption and therefore usually have the following form:

$$p(x,t) = p_o(x,t) + \sum_i g_i(t) f_i(x) \tag{9}$$

where $p_o(x,t)$ is the equilibrium (quasi-static) distribution, which is the solution of the diffusion equation with $dp/dt = 0$.

A variety of functions is used for the terms $f_i(x)$: polynomial, trigonometric, exponential, hyperbolic, etc. The $f_i(x)$ are trial functions, and the time-dependent coefficients $g_i(t)$ are determined so that a good approximation is achieved. Systematic methodologies like variational methods or the method of weighted residuals can be applied [42], [69]. They lead to a set of ordinary differential equations for the determination of $g_i(t)$. (These procedures are also used for the numerical method of finite elements.) Usually, only a few terms are included in the sum of (9) in order to limit the computation effort.

Some functions (e.g., a Fourier series with exponential time dependence of the coefficients) are particular exact solutions of the diffusion equation if specific boundary conditions (e.g., constant carrier densities at the borders) and initial conditions are fulfilled. In spite of the restrictions, they are sometimes used for the construction of a general solution.

2) Substitution in Equation: Another approach to an approximate solution is the substitution of approximating functions for the time derivative in the diffusion equation. An example [101] is

$$\frac{dp}{dt} = h(t) p(x,t). \tag{10}$$

In most cases, a sum of product terms is also used to separate variables

$$\frac{dp}{dt} = \sum_i h_i(t) f_i(x). \tag{11}$$

The substitutions transform the partial differential equation into an ordinary differential equation which can easily be solved if suitable functions are chosen. The solution of (11) has the form of (9). In the simplest case, only one term $f_i(x)$, which has in addition a linear x dependence, is used [53]. Higher accuracy is obtained with more terms $f_i(x)$ and different or variable dependences on x [75].

3) Neglecting of Terms: If the charge carrier lifetime is high, the influence of recombination on the device characteristics becomes unimportant and the term p/τ of the diffusion equation can be neglected. This equation then has the form of the heat conduction equation, and the respective solution methods can be applied [91]. However, only few devices are suited for it.

C. Transformation

There exist several mathematical techniques to solve differential equations analytically, for example, the differential equation can be transformed into an integral equation. Two methods have been used for the diffusion equation concerning power device models: Laplace transformation [116]–[122] and the application of Green's functions [123]. In principle, these methods can lead to exact solutions, however, there are constraints for the boundary conditions and the solutions consist of infinite series. Since the series must be truncated to obtain results, which are practicable and do not require too much computational effort, the solutions are approximated.

1) Laplace Transformation: The Laplace transform technique converts the diffusion equation into "s space"

$$D \frac{d^2 p'}{dx^2} = p' \left(s + \frac{1}{\tau} \right) \tag{12}$$

where $p' = p(x,t) - p(x,0)$. The solution which is converted back to the time domain consists of a Fourier series. Since a truncation after a few terms is necessary to obtain a reasonable compact model, the series should converge rapidly. But convergence and therefore the accuracy with a small number of terms depend on the boundary conditions.

This method is rigorous only if the boundaries of the considered region are fixed. This is a case which occurs only under special conditions or during a short period of the transients. In the general case, the boundaries are moving, and their movement has an important influence on the device characteristics.

The solution has the form of the approximation (9) and can therefore also be regarded as a theoretical validation of that approach.

2) Green's Function: With the help of Green's functions, a dynamic model for pn-junction diodes has been derived. This method, however, has limitations similar to those of the Laplace transformation.

D. Lumped Model

In the lumped-charge approach [124]–[133], the charge-storing region is subdivided into several sections, and the charge of each section is assigned to a charge storage node. The charge difference between two neighboring nodes determines the current. In (3), the derivative of the charge carrier densities is replaced by the difference of charges

$$qA \frac{dp}{dx} \rightarrow \frac{\Delta Q}{(\Delta x)^2}. \tag{13}$$

This leads to relative simple equations with little computation effort. The equations are valid for all stages of operation and are not limited to special cases. But only medium accuracy is achieved with a small number of nodes.

E. Numerical Solution

The most accurate solution is obtained by numerical methods, which are based on the discretization of the considered region into a finite number of mesh points. Two methods can be distinguished. However, so far mainly the first one has been applied.

1) Finite Differences: If the method of finite differences [134]–[141] is used, the derivatives in the diffusion and transport equations are expressed by differences which have the form

$$\left.\frac{dp}{dx}\right|_r = \frac{-p_{r+2} + 4p_{r+1} - 3p_r}{2\Delta x} \tag{14}$$

$$\left.\frac{d^2p}{dx^2}\right|_r = \frac{p_{r-1} - 2p_r + p_{r+1}}{(\Delta x)^2}. \tag{15}$$

The index r indicates the mesh-point number. Time is also discretized and an algebraic equation system results. The lumped-charge approach looks similar to the method of finite differences. It can be regarded as a simplification to the greatest possible extent with a minimal number of nodes. But in a lumped model, the average charge densities of the sections instead of the densities at the nodes are inserted into the equations.

2) Finite Elements: Another possible numerical approach is the method of finite elements [142], [143]. It uses mathematical functions as approximate solutions for each of the discretized regions.

IV. PARAMETERS

The accuracy of a model depends on the quality of its parameters. This topic has not been treated with sufficient attention in the case of power semiconductor models for circuit simulation so far. Only in a part of the modeling papers the required parameters are declared and methods of their determination are described [4], [9], [11]–[13], [20], [21], [23], [28], [32], [37], [38], [49], [50], [81], [83], [92], [126], [132], [133]. For single examples, excellent agreement with measurements can be obtained by adjusting the model parameters to the individual case. But for a general validity of the model and its parameters in the whole operation range, a systematic procedure of parameter extraction is necessary. Models are valuable for power circuit designers only if reliable parameter sets are provided for them.

The simpler models usually have a small set of parameters which are mainly obtained by fitting them to the observed device characteristics. The more advanced models require a larger parameter set, and since they are based on physics, their parameters mainly depend on the physics, structure, and technology of the devices.

A. Parameter Classification

1) Technological Parameters: These parameters concern the device structure and properties of the material—they are widths and areas of the different regions and the dopings of the semiconductor regions. Average doping concentrations are mainly used. In some cases, however, the knowledge about the doping profile is important.

2) Physical Parameters: These are associated with the basic physical phenomena like generation, recombination and transport of charge carriers. They are, e.g., intrinsic carrier concentration, carrier mobilities, and lifetimes. Some of them are not parameters in the narrow sense, but rather physical constants or quantities, which are determined by the semiconductor physics.

3) Electrical Parameters: These determine the electrical characteristics of the device. In many cases, they can be composed of several physical and technological parameters. Typical examples are: saturation current, breakdown voltage, threshold voltage, transconductance, current gain, capacitances (at certain voltages, e.g., 0 V), and resistances.

4) Thermal Parameters: These are used to describe the temperature effects. A part of them are the temperature coefficients of the temperature-dependent parameters. The self-heating of the device is usually modeled with the help of thermal resistances and capacitances, which are used to form a thermal network incorporating also the properties of packages as well as the heat sink.

5) Fitting Parameters: Some parameters are not deducible from the device physics. They are introduced to improve the fit of the model to the measurements. The parameters of functional models are mainly fitting parameters. But even models which are strictly based on physics can contain a few parameters of this kind. They are used to compensate inaccuracies resulting from simplifications and to optimize the results. Parameters also can lose their physical meaning and become pure fitting parameters if nonphysical values are used.

Examples of fitting parameters are ideality factors, time constants, etc.

B. Parameter Extraction

The model parameters can be obtained from several sources and by empirical as well as systematic procedures. However, the main approach is to extract them from measured device characteristics. We will discuss here this latter approach in more detail because we believe that this is the one which should be followed and toward which the efforts for necessary improvements should be directed. There are two systematic methods for parameter extraction from measured device characteristics which can be distinguished.

1) Parameter Optimization: Mathematical optimization algorithms are used to find the best fit of the model to the measured data. They are applied to a set of parameters. However, this method works well only if the parameter set is small, and it may therefore be helpful to partition the parameters into groups. The algorithms may not converge to physical values, and it may be necessary to start with suitable initial values and to bound the parameter values to their physical range.

The advantage of this method is that it can be applied to the complete device model with any set of equations.

2) Parameter Isolation: Device characteristics are selected which depend upon one or a few parameters only. From a chosen characteristic, a parameter is extracted with the help of model equations describing the respective feature. This happens in a sequential procedure—extracted parameter values are usable for further steps. But the isolation of a parameter is not always possible since several parameters can interact or the characteristics are influenced in an indirect, complicated way. A strong simplification of the model equations is often necessary to solve for the unknown parameter.

3) Discussion of Practical Parameter Extraction Strategies: Due to the mentioned problems, a combination of both extraction methods may be the advisable procedure to obtain the optimum parameter values.

The best source of the technological parameters is the device manufacturer who has all the required knowledge about them. They could also be determined by measurements, but high accuracy is obtained only with nonelectric destructive methods which require large effort.

Most of the physical parameters can be calculated or taken from graphs in textbooks. An extraction from measurements is not required. The important exception is the charge carrier lifetime which must be determined by measurements. The lifetime depends on the manufacturing process—it can vary in a wide range, and, in many cases, it has an important influence on the device characteristics. However, it is sometimes difficult to isolate it. The carrier mobilities are often treated as free parameters to obtain a better fit of the model to the measurement. But this means that they can lose their property of physical parameters.

The electrical parameters could be theoretically calculated from technological and physical parameters. However, the relations can be rather complicated and the required detailed informations are often not available. Therefore, these parameters are usually extracted from electrical measurements which often result in an increased accuracy.

Many temperature coefficients can be taken from textbooks. However, in some cases a better fit is obtained by adjustment to measurements. The thermal resistances and capacitances could be calculated from material properties of device, package, and heat sink, but due to the many simplifications made for thermal models, it is usually better to extract these parameters from measurements of the dynamic thermal characteristics.

The fitting parameters are obtained by parameter optimization methods.

The use of physics-based parameters has several advantages. The models can provide the information how the device characteristics depend on the technology, and it is possible to predict the device behavior. The influence of parameter variations due to statistical process variations can be investigated, and a “worst case” analysis can be performed.

On the other hand, it may be difficult to obtain the parameter values. The information of data sheets is not sufficient and additional dynamic measurements are necessary which, in many cases, require large effort and experience. The extraction of geometrical data and doping concentrations from electrical measurements is rather vague. The parameter spread should also be determined. This means that a large number of devices have to be investigated. Due to these problems, the conclusion is drawn that the main source of parameter information should be the device manufacturer who could most effectively provide such data.

V. EVALUATION OF THE DIFFERENT POWER SEMICONDUCTOR MODELING CONCEPTS FOR CIRCUIT SIMULATION

Although we try to perform this evaluation of the different concepts as far as possible on an objective basis, an inclusion of some subjective views and judgements of the authors is of course unavoidable. Therefore, the opinion of the authors is reflected to some extent in the presented material and the conclusions.

A. Criteria for Comparison and Evaluation

Within each of the different modeling concepts there are, of course, certain degrees of freedom with respect to a tradeoff between different contradicting model requirements. For example, it would be possible within all modeling concepts to place the main emphasis on the accuracy of the solution obtained for the switching waveform. To achieve improvements with respect to this quality feature of the circuit simulation model, a tradeoff has to be performed with respect to other quality features of the same circuit simulation model, as, e.g., the required calculation time or simplicity of parameter determination. Nevertheless, principle boundaries for freedom with respect to such tradeoffs are narrower for some of the modeling concepts and wider for others. This results from a different interdependence between the various criteria when different modeling concepts are used. For an overall comparison of the different modeling concepts, these possibilities for tradeoff have to be taken into account, and it has to be evaluated what can be achieved with each modeling concept on an equivalent basis.

In our evaluation of the different modeling concepts, we try to apply the following five criteria: 1) accuracy of predicted solutions, with respect to the functionality of power circuits; 2) required computation power, to achieve comparable results; 3) feasibility and simplicity of parameter determination; 4) limitations in the possibilities for a broad application; and 5) anticipated potential for future development and refinement of the concept. These criteria are, of course, interdependent in a complex way and also have some overlap in meaning. In applying them, some subjectiveness is inevitable, to reach to a final judgement and conclusion. From the evaluation procedure in this sense, the main application target of each of the modeling concepts will also emerge in a natural way.

B. Methods for Implementation into a Circuit Simulator

There are a variety of commercial circuit simulation programs (SPICE, SABER, and ELDO) available on the market. In addition, a number of proprietary circuit simulation programs of large industrial companies (PSTAR, TITAN, and ASTAP) exist as well. All of these simulation programs differ in particular in the possibilities and methods they provide for the implementation of new device models. The spectrum

TABLE III
EVALUATION OF MODELING CONCEPTS (1 = EXCELLENT, 5 = POOR)

	Exactness	Calculat. Time	Parameter Determin.	Application Limits	Future Potential	Main Target	Published Literature
Functional Model	5	2	1	4	4	large circuits, system level	[3-40]
Approxim. Solution	2	3	3	2	2	medium circuits	[41-115]
Trans-formation	2	3	3	5	5	medium circuits	[116-123]
Lumped Model	4	1	2	3	2	large circuits	[124-133]
Numerical Solution	1	5	5	1	1	small circuits	[134-143]

extends here from a fixed set of functional elements (e.g., passive components like resistors, capacitors, inductances—active components like conventional diodes, MOSFET's, bipolar transistors, or general elements like controlled voltage and current sources), which must be used to construct the new device models on one hand up to the possibility for implementation of mathematical relationships like differential equations and implicit functions or even complete subroutine programs on the other hand. Therefore, implementation methods into a circuit simulator depend on what that special simulator has to offer. This can mean in particular that a certain modeling concept cannot be put into reality with a given circuit simulation program. We distinguish two main methods—the subcircuit and mathematical implementation methods, which have been used in the past to implement power semiconductor device models into circuit simulation programs. The mathematical method is generally applicable to all modeling concepts and the subcircuit method with its inherent demerits in flexibility to most of them.

1) The Subcircuit Implementation Method: Originally, circuit simulation programs (like SPICE and its derivatives) have not been written to serve the needs of designing power electronic circuits, but to serve the needs of designing low-power and low-voltage electronic circuits monolithically integrated on silicon chips as well as manufactured on printed circuit boards. These circuit simulation programs have become widely used among electrical engineers and have been accepted as standard low-cost working tools. In addition, service and maintenance are provided by a number of commercial vendors. However, nearly all of the widespread low-cost circuit simulation programs restrict themselves to a fixed set of functional elements (as outlined above, e.g., passive components, active components, and, in addition, controlled voltage and current sources) and do not allow user-defined functional elements except for a combination of these fixed functional elements into subcircuits. The subcircuit implementation method tries to accept these restrictions of widespread circuit simulation programs for the implementation of a new power semiconductor device model.

Unfortunately, the subcircuit implementation of accurate solutions for modeling power semiconductor devices soon becomes very complex. The reason for this fact is that the complex physical processes in the semiconductor device have to be imitated by a combination of in principle inappropriate elements. An unfavorable balance between accuracy and required computation power results and is unavoidable in principle. Therefore, applicability and also future development of the subcircuit implementation are expected to be rather limited. On the other hand, one great advantage is connected with the restrictions of this implementation method and makes it attractive despite of all its demerits. The resulting models can be implemented in nearly every available circuit simulator and therefore have the best chances to become widely used if they can be tailored to do the required job.

2) The Mathematical Implementation Method: If the circuit simulation program offers the individual definition of device models by describing them in mathematical form in a special description language or by writing a program in a general-purpose programming language, the mathematical implementation method can be used. This method is, of course, most effective with respect to modeling the unique physical phenomena present in power semiconductor devices because the mathematical relationships can be implemented directly in the form of the chosen approximation or solution. The demerit of the mathematical implementation method comes from the fact that the usability of the resulting power semiconductor device model is automatically restricted to normally just one circuit simulation program, which is often quite expensive.

The most straightforward mathematical model implementation would result for a lookup table model, again from the group of functional modeling concepts.

C. Detailed Discussion of Merits and Demerits of the Different Modeling Concepts

In the following, we will apply the criteria outlined above to an analysis and discussion of the modeling concepts identified in Section III. For most of the different modeling concepts, the implementation forms of subcircuits as well as mathematical models are possible in principle. Only lookup tables (subgroup of functional models) and numerical concepts clearly require a mathematical implementation. An overview of our evaluation is given in Table III and has the form of a ranking of the different modeling concepts with respect to our criteria.

1) Functional Models: This class of models is especially suited for specific applications, where the tasks consist of dimensioning and characterizing power circuits, which, e.g., all have a similar basic topology. In such a case, it is not necessary to have a large portion of the power semiconductor device physics implemented into the model. It is most likely sufficient to imitate the behavior of the power semiconductor device within the special circuit topology by adjusting the parameters of selected mathematical expressions by storing the behavior in lookup tables or even by using parameter fitted low-power device models. In this way, the speed advantages of functional models can be exploited without sacrificing to much in exactness of the circuit simulation result. However, functional models come to their limits if it is intended to use them for a new circuit topology, while still keeping the parameters determined for the old circuit topology. In such a case, the differences between the real device behavior and the simulation results are expected to show up especially in the dynamic properties of the switching process. Therefore, usually new model parameters have to be determined for each new circuit topology.

Other application fields of functional models are the cases where previously simple switching models (linear or abrupt change of state) with a fixed resistance in the conducting state have been sufficient. These are the applications with low switching frequencies or with a large number of single power semiconductor device elements. Here, either the exact reproduction of the switching characteristics is of lower order importance and/or the high calculation speed, which functional models are able to offer, is a must.

In an overall judgement, the future potential of functional models of power semiconductor devices for circuit simulation is regarded as rather limited. Because of their deficits in accuracy, they will be replaced by models based on other modeling concepts as soon as these models fulfill the requirements on calculation speed and practical usability. Therefore, we expect functional models to serve in future mainly the niches of some specialized applications and of very large circuits, where other modeling concepts cannot provide practical calculation times for a complete circuit simulation.

We expect, however, that functional models have their main application area on the level of complete system simulations and not on the level of circuit simulation. Here, the merits of functional models come to their full strength, whereas their deficits are of lower order importance.

2) Approximate Solution: Within the framework of this modeling concept, substantial improvements in the state of the art of power semiconductor device models for circuit simulation have been achieved in recent years. The basic power device phenomena with respect to resistivity modulation, charge storage, MOS capacitances, breakdown, and even electrothermal interaction could be implemented in a physical way and at a reasonable cost of computation power. In the meantime, models for all main types of power semiconductor devices (power diode, power bipolar transistor, power MOSFET, IGBT, thyristor, GTO, and MCT) exist and are in practical use.

Naturally, a very wide span of approximations and simplifications, as outlined in Section III, is possible in principle. These approximations may be chosen very near to analytical solutions on one hand or very far from analytical solutions on the other hand. In our view, only those approximations, which come very near the exact solutions of the underlying physical relationships are promising for the future development of power semiconductor device models for circuit simulation. Otherwise, a functional model would be the right choice and strategy from the beginning. Most of the recent contributions, which employ an approximate solution according to our classification, indeed use approximations coming very near to an exact solution of the physical equations.

Due to the physical nature of the resulting power device models, their application to nearly all problems in power circuit design seems to be possible. The main exception to this general statement are predominantly analog applications, where specific further refinements of the existing approximations would be necessary. The required model parameters are mainly of geometrical and physical nature. The parameter determination for a given power device needs some effort, but is judged to be of manageable difficulty in practical cases. Because of the outlined advantages and the proven applicability in practical cases, approximate solutions are a quite promising direction for future research and practical employment of power device models for circuit simulation. A successful implementation into a circuit simulation program seems to be only meaningful if the mathematical implementation method can be used. The application field, for which this modeling concept of power semiconductor devices is in our opinion most appropriate, is the design of power electronic circuits with a medium number of components.

3) Transformation: Many of the statements, which are true for the modeling concept of approximate solutions, are in our judgment also true for this modeling concept, which after the transformation procedure normally also results in a final approximation. However, the exact solution (at least for a chosen boundary condition) is kept during the whole transformation procedure. The main purpose of the transformation is to enlarge the chances for finding an exact solution or to facilitate at least the search for a nearly exact solution. Since the transformation normally results in a series of terms with decreasing importance, the quality of the chosen transformation is revealed by the speed of convergence of this series, which has to be truncated to be practically applicable.

Because there exist only few publications in which the transformation concept has been used to construct power semiconductor device models, the usefulness of this concept is verified to a much lower degree as, e.g., for the concept of approximate solutions. In this context, the most important questionable issue is moving boundaries of the crucial power semiconductor device region to which the transformation has to be applied. Up to now, it has to our knowledge not been shown that the transformation concept is capable of successfully treating moving boundaries, which is most important for correctly describing the phenomena of conductivity modulation and charge storage.

Nevertheless, we expect that a wider application of the transformation concept for developing power semiconductor models is possible and may in the future be demonstrated by the research groups working with this concept. The proper application area is most likely also the design of power electronic circuits with a medium number of components.

4) Lumped Model: Lumped models offer in our view a favorable tradeoff between calculation speed and accuracy, which emphasizes the requirements of calculation speed. The concept of lumped models has been demonstrated to be capable of modeling, at least with a moderate degree of accuracy, the important features of the basic physical phenomena, occurring especially in power semiconductor devices.

Normally, only a few parameters are necessary, which are in close relation with the electrical characteristics of the power semiconductor device. Therefore, the parameter determination is judged to be comparatively uncomplicated and straightforward.

In our opinion, lumped models are one of the new important directions of power semiconductor device modeling, which are expected to show considerable future development and which are expected to have their main strength in the simulation of power electronic circuits with a large number of components.

5) Numerical Solution: Numerical modeling concepts incorporate the possibility to perform the tradeoff toward highest accuracy at the cost of mainly the calculation speed. In the same way, as functional models must be viewed at the border to the modeling concepts for system simulation, numerical modeling concepts are located at the border to modeling concepts for device simulation. Especially in cases, where multidimensional approaches are chosen, the application area of circuit simulation is in our view clearly left and a similar computational effort, typical for a device simulation, is spent.

However, this point of view may change in future if computer technology continues to develop toward ever increasing computational power at continuously decreasing costs. In such a case, the most efficient and rational tradeoff in developing power semiconductor models for circuit simulation may be to go to increased accuracy at the cost of the required increased computational power, which numerical solutions are able to offer in a straightforward and probably also most efficient way. Substantial progress in this direction has been achieved in recent years.

Nevertheless, it is our opinion that the computational effort with a numerical model is always higher than with one of the other discussed modeling concepts if these concepts can provide the necessary level of accuracy. On the other hand, a numerical concept has the capability to go clearly beyond the accuracy of all other known modeling concepts.

Parameter determination for numerical models is judged to be also more difficult, than in the case of other modeling concepts. The main reason for this difficulty comes from the fact that numerical modeling concepts directly implement the physical relationships and are therefore nearest to the physics of power semiconductor devices. A close orientation toward the physics requires, however, a very intimate knowledge about the power semiconductor device with respect to, e.g., used materials, doping profiles, manufacturing process, and geometries, which only the manufacturer of the power semiconductor device is able to provide with a sensible effort. Of course, the high accuracy of a numerical model becomes effective only if the parameter determination is performed carefully and precisely. In addition, modeling features, which are unique for the numerical concept, like, e.g., position dependent parameters, must be exploited systematically to achieve the superiority in accuracy for a practical case.

If the outlined difficulties of numerical models can be overcome in an effective and favorable way, applicability of numerical models to all practical cases of circuit simulation is possible and has been partly demonstrated in the past. With the anticipated substantial future increase in available computational power, a high future potential for further development toward practical use in circuit simulation is predicted for power semiconductor device models based on the numerical modeling concept. However, the main application target will in our view still be power electronic circuits with a small number of components.

VI. DISCUSSION AND CONCLUSION

The art of power semiconductor device modeling for circuit simulation is at present in a status of rapid development toward increasing professionalism and applicability for practical use.

In recent years, several research groups all over the world have explored new concepts for constructing and providing power semiconductor device models, which serve the practical needs of the power electronics engineer, to design power electronic circuits with increased efficiency.

Three modeling concepts which we termed: 1) approximated solutions; 2) lumped models; and 3) numerical solutions have emerged and have been proven successful. These modeling concepts are now competing for the leading position in providing the best value for practical applications. As has been outlined in Section V, the original fields of strength for the models, resulting from these three modeling concepts, must be attributed to different complexities of the power electronic circuits under consideration, namely: 1) medium number; 2) large number; and 3) small number of components. Whether one of the modeling concepts can be further developed to enlarge its field of strength and can be proven superior, or whether they continue to exist successfully in parallel, is not clear at the moment. It, of course, depends to a large extent on the efforts and the ingenuity of the researchers working with these modeling concepts.

However, there are also additional driving forces, which come from the area of power circuit applications, manufacturers of power semiconductor devices, and developments in separate research fields, predominantly the field of computational technologies. These driving forces may implement important boundary conditions for the future development in the field of power semiconductor device models for circuit simulation.

From the application area, which is represented by the engineers who actually design the power circuits, requirements with respect to, e.g., the degree of accuracy versus calculation speed, which must be provided by useful models for circuit simulation, should be specified. If this process of specification does not proceed in an organized and well-planned way, it will nevertheless happen, but now in a more accidental way through the habits and individual decisions of power circuit designers. Such an accidental procedure may lead to temporarily wrong developments and certainly slow down the overall future progress and the practical acceptance for already achieved improvements. Clearly, it would be most effective if the end users of power semiconductor device models for circuit simulation, could channel the ongoing efforts throughout the world in such a way that they finally serve their real needs for efficient power circuit design in the best possible way. Thus, important and useful boundary conditions for future research would be provided.

As outlined in Section IV, parameter determination is one of the remaining critical issues for power semiconductor device models, which will require increased attention in future. Especially for applying the modeling concepts, which allow a higher degree of accuracy, an intimate knowledge about the individual power device is needed. Here, the manufactures for power devices play the key role. Their willingness and ability to supply information, which is necessary for parameter determination of power semiconductor device models, will also set at least implicit boundary conditions for future developments in the state of the art. One possibility for the device manufacturer, which avoids the undesired necessity to make too much proprietary information public, is to supply high-quality circuit simulation models for his product line of power devices by himself.

Another set of important boundary conditions for future development will be given by the available computational power, which fits into the development budget of the user. In the past, the resources of available computational power in this sense have been steadily increasing. If this development continues, it will clearly favor the concepts of approximate and numerical solutions. In our opinion, the issue of available computational power will finally settle the question, which one of the competing modeling concepts is going to dominate the field of circuit simulation in future. However, a dominating role of, e.g., numerical concepts in circuit simulation, would clearly not make the other modeling concepts obsolete. It would in our opinion just mean that computational power becomes so abundant that lumped models and approximate models are able to migrate to the level of power system simulation.

In conclusion, we would like to emphasize that the current speed improvements and the abundance of possible future directions for successful development make it easy to predict that a number of surprises are going to be ahead in the field of power semiconductor device models for circuit simulation.

REFERENCES

[1] P. O. Lauritzen, "Power semiconductor device models for use in circuit simulators," in *Conf. Rec. IAS'90*, pp. 1559–1563.

[2] ——, "Simulation and modeling for power electronics," in *IEEE Workshop Computers in Power Electronics*, 1988, pp. 37–42.

[3] A. Agbossou, I. Rasoanarivo, and B. Davat, "Comparative study of high power IGBT model behavior in voltage source inverter," in *PESC'96 Rec.*, pp. 56–61.

[4] S. Musumeci, A. Raciti, M. Sardo, F. Frisina, and R. Letor, "PT-IGBT PSPICE model with new parameter extraction for life-time and epy dependent behavior simulation," in *PESC'96 Rec.*, pp. 1682–1688.

[5] J. T. Hsu and K. D. T. Ngo, "A behavioral model of the IGBT for circuit simulation," in *PESC'95 Rec.*, pp. 865–871.

[6] T. Ise, H. Ishida, and Y. Murakami, "Circuit simulation of power converters considering switching characteristics of GTO's," in *Proc. IPEC-Yokohama'95*, pp. 238–243.

[7] Z. Li, C. Jiang-Yie, Z. Liang-Bing, H. Ying-Duo, W. Zhong-Hong, Z. Qing-Xiang, and H. Chao-Feng, "Transient modeling of gate turn-off thyristor using PSPICE in power electronic simulations," in *Proc. IPEC Yokohama'95*, pp. 244–248.

[8] H. A. Mantooth, R. G. Perry, and J. L. Duliere, "A unified diode model for circuit simulation," in *PESC'95 Rec.*, pp. 851–857.

[9] J. L. Duliere, H. A. Mantooth, and R. G. Perry, "A systematic approach to power diode characterization and model validation," in *Conf. Rec. IAS'95*, pp. 1069–1075.

[10] K. J. Tseng, J. Yang, C. F. Foo, M. Vilathgamuwa, and P. R. Palmer, "Performance of power diode model for circuit simulation," in *Proc. 1995 Int. Conf. Power Electronics and Drive Syst.*, pp. 519–524.

[11] T. Bonafe, S. El Baroudi, F. Bernot, and A. Berthon, "IGBT model for power electronics simulation," in *Proc. EPE'95*, pp. 1.141–1.145.

[12] J. Pilacinski, "A method for determining the parameters of power MOSFET and IGBT transistor models applied in the PSPICE program," in *Proc. EPE'95*, pp. 1.268–1.272.

[13] A. F. Petri and C. Hymowitz, "A SPICE model for IGBT's," in *Proc. APEC'95*, pp. 147–152.

[14] V. M. Guzman and M. I. G. de Guzman, "A modified J3 model for GTO simulation with SPICE," in *Proc. EPE'95*, pp. 1.216–1.221.

[15] ——, "A GTO modular macromodel for use in circuit simulation with SPICE," in *Proc. APEC'94*, pp. 1059–1065.

[16] K. J. Tseng, C. F. Foo, and P. R. Palmer, "Implementing power diode models in PSPICE and SABER," in *PESC'94 Rec.*, pp. 59–63.

[17] A. T. Yang, Y. Liu, and J. T. Yao, "An efficient nonquasi-static diode model for circuit simulation," *IEEE Trans. Computer-Aided Design*, vol. 13, no. 2, pp. 231–239, 1994.

[18] M. E. Clarke and S. Rahim, "A nonquasistatic empirical model of the power PIN diode for circuit simulation," *Int. J. Computat. Math. Electr. Electron. Eng.*, vol. 13, no. 4 , pp. 831–844, 1994.

[19] D. M. Smith, C. J. Goodman, and H. Zelaya, "GTO thyristor modeling using SABER," in *IEE Colloquium on Power Electronics and Computer Aided Engin.*, 1994, pp. 1–4.

[20] H. S. Kim, Y. H. Cho, S. D. Kim, Y. I. Choi, and M. K. Han, "Parameter extraction for the static and dynamic model of IGBT," in *PESC'93 Rec.*, pp. 71–74.

[21] Z. Shen and T. P. Chow, "Modeling and characterization of the insulated gate bipolar transistor (IGBT) for SPICE simulation," in *Proc. ISPSD'93*, pp. 165–170.

[22] D. M. Smith, H. Zelaya, and C. J. Goodman, "Implementation, characterization and refinement of a GTO model," in *5th Europ. Conf. Power Electronics and Applications*, 1993, pp. 238–243.

[23] C. Alonso, T. A. Meynard, H. Foch, C. Batard, and H. Piquet, "A model of GTO compatible with power circuit simulation," in *5th Europ. Conf. Power Electronics and Applications*, 1993, pp. 232–237.

[24] F. Bertha, B. Velaerts, P. Mathys, E. Tatakis, A. Wyns, D. Bogaerts, and M. Miller, "An improved power diode model for PSPICE, applied to converter simulation," in *5th Europ. Conf. Power Electronics and Applications*, 1993, pp. 249–254.

[25] Y.-Y. Tzou and L.-J. Hsu, "A practical SPICE macro model for the IGBT," in *Proc. IECON'93*, pp. 762–766.

[26] M. Andersson, P. Kuivalainen, and H. Pohjonen, "Circuit simulation models for MOS-gated power devices: Application to the simulation of an electronic lamp ballast circuit," in *Proc. IEEE APEC'93*, pp. 498–503.

[27] E. Tatakis, "Modeling power diodes for power electronic circuits simulation with SPICE2," *EPE J.*, vol. 2, no. 4, pp. 259–260, 1992.

[28] M. Melito and F. Portuese, "A new approach to parameter extraction for SPICE power MOSFET model," in *Proc. EPE-MADEP'91*, pp. 301–305.

[29] W. J. Hepp and C. F. Wheatley, "A new SPICE sub-circuit for the power MOSFET featuring global temperature options," in *PESC'91 Rec.*, pp. 533–544.

[30] F. Wheatley, H. Ronan, and G. Dolny, "Modified SPICE II models modern power MOSFET's," *Electron. Prod. Design*, vol. 8, no. 7, pp. 25–26, 1987.

[31] G. M. Dolny, H. R. Ronan, and C. F. Wheatley, "A SPICE II subcircuit representation for power MOSFET's using empirical methods," in *Proc. Power Electronics Design Conf.*, 1985, pp. 147–153.

[32] K. Shenai, "A circuit simulation model for high-frequency power MOSFET's," *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 539–547, 1991.

[33] C. L. Tsay, R. Fischl, J. Schwartzenberg, H. Kan, and J. Barrow, "A high power circuit model for the gate turn off thyristor," in *PESC'90 Rec.*, pp. 390–397.

[34] Y. C. Liang and V. J. Gosbell, "Diode forward and reverse recovery model for power electronic SPICE simulations," *IEEE Trans. Power Electron.*, vol. 5, no. 3, pp. 346–356, 1990.

[35] A. Vladimirescu and M. Walker, "A power MOSFET macro-model for circuit simulation," in *Proc. PCIM'90*, pp. 85–91.

[36] A. Brambilla and E. Dallago, "Three-junction device simulation model," *Electron. Lett.*, vol. 25, no. 14, pp. 936–937, 1989.

[37] J. M. Hancock, "A MOSFET simulation model for use with microcomputer SPICE circuit analysis," in *Proc. 16th Int. PCI'88 Conf.*, pp. 276–289.

[38] J. M. Hancock, "A MOSFET simulation model for use with microcomputer SPICE circuit analysis," in *Proc. 14th Int. PCI'87 Conf.*, pp. 282–295.

[39] J. C. Freire, "A MOS power transistors model for SPICE2G," in *Proc. MELECON'85*, vol. 3, pp. 1–4.

[40] P. Antognetti, B. Cotta, B. Gabriele, G. Massobrio, and G. Sciutto, "Modeling and simulation of power transistors in electronic power converters," in *EUROCON'80*, pp. 367–369.

[41] B. Fatemizadeh, G. Tchouangue, and D. Silber, "A user-optimized electrothermal IGBT model for power electronic circuit simulation in the circuit simulator ELDO," in *Proc. IEEE APEC'96*, pp. 81–87.

[42] B. Fatemizadeh and D. Silber, "A versatile electrical model for IGBT including thermal effects," in *PESC'93 Rec.*, pp. 85–92.

[43] P. Lethurcq, O. Berraies, and J. L. Massol, "Implementation and validation of a new power diode model for circuit simulation," in *PESC'96 Rec.*, pp. 35–43.

[44] P. Leturcq, O. Berraies, J. L. Debrie, P. Gillet, M. A. Kallala, and J. L. Massol, "Bipolar semiconductor device models for C.A.D. in power electronics," in *Proc. EPE'95*, pp. 1.222–1.227.

[45] A. R. Hefner, "Modeling buffer layer IGBT's for circuit simulation," *IEEE Trans. Power Electron.*, vol. 10, no. 2, pp. 111–123, 1995.

[46] ——, "A dynamic electrothermal model for the IGBT," *IEEE Trans. Ind. Applicat.*, vol. 30, no. 2, pp. 394–405, 1994.

[47] C. S. Mitter, A. R. Hefner, D. Y. Chen, and F. C. Lee, "Insulated gate bipolar transistor (IGBT) modeling using IG-SPICE," *IEEE Trans. Ind. Applicat.*, vol. 30, no. 1, pp. 24–33, 1994.

[48] A. R. Hefner and D. M. Diebolt, "An experimentally verified IGBT model implemented in the Saber circuit simulator," *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 532–542, 1994.

[49] A. R. Hefner, "Modeling power semiconductor devices for realistic simulation," in *IEEE 4th Workshop Computers in Power Electronics*, 1994, pp. 11–44.

[50] ——, "Modeling buffer layer IGBT's for circuit simulation," in *PESC'93 Rec.*, pp. 60–69.

[51] ——, "A dynamic electrothermal model for the IGBT," in *Conf. Rec. IAS'92*, pp. 1094–1104.

[52] A. Hefner and D. M. Diebolt, "An experimentally verified IGBT model implemented in the Saber circuit simulator," in *PESC'91 Rec.*, pp. 10–19.

[53] A. R. Hefner, "An improved understanding for the transient operation of the power insulated gate bipolar transistor (IGBT)," *IEEE Trans. Power Electron.*, vol. 5, no. 4, pp. 459–468, 1990.

[54] ——, "Analytical modeling of device circuit interactions for the insulated gate bipolar transistor (IGBT)," *IEEE Trans. Ind. Applicat.*, vol. 26, no. 6, pp. 995–1005, 1990.

[55] ——, "Analytical modeling of device circuit interactions for the insulated gate bipolar transistor (IGBT)," in *Conf. Rec. IAS'88*, pp. 606–614.

[56] A. R. Hefner and D. L. Blackburn, "An analytical model for the steady-state and transient characteristics of the power insulated gate bipolar transistor," *Solid-State Electron.*, vol. 31, pp. 1513–1532, 1988.

[57] R. Dutta, C. Tsay, A. Rothwarf, and R. Fischl, "A physical and circuit level approach for modeling turn-off characteristics of GTO's," *IEEE Trans. Power Electron.*, vol. 9, no. 6, pp. 560–566, . 1994.

[58] K. J. Tseng and P. R. Palmer, "Modeling of power semiconductor devices for use in circuit simulations," in *PESC'94 Rec.*, pp. 38–43.

[59] ——, "Mathematical model of gate-turn-off thyristor for use in circuit simulations," *Proc. Inst. Elect. Eng.*, vol. 141, no. 6, pp. 284–292, 1994.

[60] T. Maurel, R. Bouchakour, and C. Lallement, "One-dimensional model of the power bipolar transistor with thermoelectrical interactions for circuit applications," in *1995 IEEE Symp. Circuits and Syst.*, pp. 1860–1863.

[61] ——, "Modeling the electrothermal behavior of the power bipolar transistor," in *PESC'95 Rec.*

[62] ——, "Modeling the electrothermal behavior of the power bipolar transistor," in *Proc. IPEC-Yokohama'95*, pp. 1244–1249.

[63] ——, "Modeling and simulation of the electrothermal behavior of the power bipolar transistor," in *Proc. 1995 Int. Conf. Power Electronics and Drive Systems*, pp. 281–286.

[64] B. Allard, H. Morel, C. C. Lin, H. Helali, and J. P. Chante, "Rules for deriving basic semiconductor region models," in *PESC'94 Rec.*, pp. 44–51.

[65] H. Morel, S. H. Gamal, and J. P. Chante, "State variable modeling of the power pin diode using an explicit approximation of semiconductor device equations," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 112–120, Jan. 1994.

[66] C. Lallement, R. Bouchakour, and T. Maurel, "One-dimensional analytical modeling of the VDMOS transistor taking into account the thermoelectrical interactions," in *Proc. 37th Midwest Symp. Circuits and Syst. 1994*, pp. 682–687.

[67] ——, "A VDMOS transistor model taking into account the thermoelectrical interactions," *1994 IEEE Int. Symp. Circuits and Syst.*, vol. 1, pp. 327–330.

[68] B. Allard, H. Morel, and J. P. Chante, "Reusing basic semiconductor region models in power device bond graph definition," in *5th Europ. Conf. Power Electronics and Applications*, 1993, pp. 34–39.

[69] ——, "State-variable modeling of high level injection regions in power devices," in *PESC'92 Rec.*, pp. 885–892.

[70] T. Kern, R. Kraus, and K. Hoffmann, "A precise analytical model for diffused power diodes," in *Proc. EPE'95*, pp. 1.146–1.150.

[71] M. Bayer, R. Kraus, and K. Hoffmann, "A new analytical GTO model for circuit applications," in *PESC'95 Rec.*, pp. 879–885.

[72] R. Kraus, K. Hoffmann, and P. Tuerkes, "Analysis and modeling of the technology-dependent electrothermal IGBT characteristics," in *Proc. IPEC-Yokohama'95*, pp. 1133–1138.

[73] M. Bayer, R. Kraus, and K. Hoffmann, "A precise model for the dc and transient characteristics of BJT's," in *PESC'94 Rec.*, pp. 64–68.

[74] R. Kraus and K. Hoffmann, "An analytical model of IGBT's with low emitter efficiency," in *Proc. ISPSD'93*, pp. 30–34.

[75] R. Kraus, K. Hoffmann, and H. J. Mattausch, "A precise model for the transient characteristics of power diodes," in *PESC'92 Rec.*, pp. 863–869.

[76] R. Kraus, P. Tuerkes, and H. J. Mattausch, "Modeling the self-heating of power devices," in *Proc. ISPSD'92*, pp. 124–129.

[77] R. Kraus, K. Hoffmann, and P. Tuerkes, "Reverse recovery model of power diodes," in *Proc. EPE-MADEP'91*, pp. 343–345.

[78] S. Winternheimer, "Investigations on the turn-on process in fast recovery diodes," in *Proc. EPE-MADEP'91*, pp. 119–124.

[79] Y. Jin, K. Hoffmann, and W. Kiffe, "A forward recovery model of power diodes," *EPE-MADEP'91 Proc.*, pp. 339–342.

[80] G. Busatto, "Physical modeling of bipolar mode JFET for CAE/CAD simulation," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 368–375, 1993.

[81] Y. C. Liang and V. J. Gosbell, "Transient model for gate Turn-off-Thyristor in power electronic simulations," *Int. J. Electron.*, vol. 70, no. 1, pp. 85–99, 1991.

[82] Y. Kawaguchi, Y. Terazaki, and A. Nakagawa, "Subcircuit SPICE modeling of a lateral IGBT for high voltage power IC design," in *Proc. ISPSD'95*, pp. 346–349.

[83] M. Kimata, M. Koyama, R. Uchida, M. Ikeda, T. Kawamura, and T. Okada, "Smart IGBT model and its application for power converter design," in *Conf. Rec. IAS'94*, pp. 1168–1173.

[84] Z. Shen and T. P. Chow, "An analytical IGBT model for power circuit simulation," in *Proc. ISPSD'91*, pp. 79–82.

[85] K. Grahn, S. Eranen, A. Heuberger, and H. Ryssel, "An analytical model for the vertical insulated gate bipolar transistor," in *Proc. ESSDERC'89*, pp. 431–434.

[86] J. G. Fossum and Y.-S. Kim, "Static and dynamic latchup in the LIGBT," *IEEE Trans. Electron Devices*, vol. 35, no. 11, pp. 1977–1985, 1988.

[87] J. G. Fossum, R. J. McDonald, and M. A. Shibib, "Network representation of LIGBT structures for CAD of power integrated circuits," *IEEE Trans. Electron Devices*, vol. 35, no. 4, pp. 507–515, 1988.

[88] D. S. Kuo and C. Hu, "An analytical model for the power bipolar-MOS transistor," *Solid-State Electron.*, vol. 29, pp. 1229–1237, Dec. 1986.

[89] R. A. Wunderlich and P. K. Ghosh, "Modeling the gate more accurately for power MOSFET's," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 105–111, 1994.

[90] N. Andersson, M. Gronlund, P. Kuivalainen, and H. Pohjonen, "A comparative study of physical and subcircuit models for MOS-gated power devices," in *Proc. ISPSD'94*, pp. 315–320.

[91] P. Tuerkes and R. Kuhnert, "Compact models for the circuit simulation of power semiconductors," in *6th Int. Conf. Power Semiconductors and Their Applications*, Munich, Germany, 1992, pp. 17–25.

[92] P. Tuerkes and H. J. Mattausch, "A new generation of circuit simulators makes power MOSFET models simple," in *Proc. EPE-MADEP'91*, pp. 276–279.

[93] M. Napieralska, H. Tranduc, C. E. Cordonnier, J. P. Berry, and P. Rossel, "Power MOSFET's library builder for switching circuits simulation and design," in *Proc. EPE-MADEP'91*, pp. 295–300.

[94] W. Soppa and J. Haenseler, "A process oriented VDMOSFET model for circuit simulation," in *Proc. ISPSD'92*, pp. 184–187.

[95] N. S. Dogan and E. Lozano, "A new device model of VDMOSFET for SPICE simulations," in *Proc. ISPSD'91*, pp. 84–88.

[96] I. Budihardjo and P. O. Lauritzen, "Performance requirements for power MOSFET models," in *PESC'94 Rec.*, pp. 69–76.

[97] C. K. Ong, P. O. Lauritzen, and I. Budihardjo, "A mathematical model for power MOSFET capacitances," in *PESC'91 Rec.*, pp. 423–429.

[98] P. O. Lauritzen, J. Ong, and C. L. Ma, "Power MOSFET and power diode models," in *IEEE Workshop Computers in Power Electronics*, 1990, pp. 245–249.

[99] K. H. Lou, C. M. Liu, and J. B. Kuo, "An analytical quasisaturation model for vertical DMOS power transistors," *IEEE Trans. Electron Devices*, vol. 40, no. 3, pp. 676–679, 1993.

[100] M. Stiftinger and S. Selberherr, "An analytical dc- and ac-model for vertical smart power DMOS transistors," in *Int. Seminar on Power Semiconductors*, Prague, Czechoslovakia, 1992, pp. 89–93.

[101] C. H. Xu and D. Schroeder, "A power bipolar junction transistor model describing static and dynamic behavior," *IEEE Trans. Power Electron.*, vol. 7, no. 4, pp. 734–740, 1992.

[102] K. Reinmuth and C. H. Xu, "Experimental investigation, simulation and analyzes of avalanche effects on power MOSFET's," in *PESC'90 Rec.*, pp. 120–125.

[103] C. H. Xu and D. Schroeder, "A unified model for the power MOSFET including the inverse diode and the parasitic bipolar transistor," in *Proc. EPE'89*, pp. 139–143.

[104] Y. S. Kim and J. G. Fossum, "Physical DMOST modeling for high-voltage IC CAD," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 797–803, 1990.

[105] G. A. Franz, J. P. Walden, R. S Scott, W. H. Bicknell, and R. L. Steigerwald, "Use of accurate MOS models for optimizing resonant converter designs," in *Conf. Rec. IAS'90*, pp. 1564–1568.

[106] R. S. Scott and G. A. Franz, "An accurate model for power DMOSFET's including interelectrode capacitances," in *PESC'90 Rec.*, pp. 113–119.

[107] G. A. Franz, "Efficient and accurate circuit modeling of power DMOSFET's," in *Proc. NASECODE VI*, 1989, pp. 108–113.

[108] J. G. Fossum and R. J. McDonald, "High-voltage device modeling for SPICE simulation of HVIC's," *IEEE Trans. Computer-Aided Design*, vol. 7, pp. 425–432, Mar. 1988.

[109] C. E. Cordonnier, R. Maimouni, M. Belabadia, P. Rossel, H. Tranduc, and D. Allain, "SPICE model for power MOSFET's working on both resistive and inductive switching tests," in *Proc. 1st Int. PCIM'88*, pp. 229–242.

[110] F. X. Timmes, D. T. Dodt, and N. Maluf, "Circuit simulation of power MOSFET's," in *Conf. Rec. 1986 IAS*, pp. 393–395.

[111] X. He, B. W. Williams, and T. C. Green, "Power switching semiconductor models for PSpice, and their parametric sensitivity analysis," in *IEE 5th Int. Conf. Power Electronics and Variable-Speed Drives*, 1994, pp. 543–549.

[112] ——, "Composite power switching semiconductor models and their parametric sensitivity analysis," in *Proc. IPEMC'94*, Beijing, China, pp. 188–194.

[113] B. W. Williams, "Power semiconductor device modeling," *J. Electr. Electron. Eng.*, vol. 4, no. 3, pp. 239–249, 1984.

[114] ——, "Computer modeling of power thyristor circuits," in *EUROCON'80*, pp. 370–373.

[115] B. E. Danielsson, "Studies of turn-off effects in power semiconductor devices," *Solid-State Electron.*, vol. 28, no. 4, pp. 375–391, 1985.

[116] A. G. M. Strollo, "SPICE modeling of power pin diode using asymptotic waveform evaluation," in *PESC'96 Rec.*, pp. 44–50.

[117] A. G. M. Strollo and P. Spirito, "A new pin diode modeling approach for power electronic PSPICE simulations," in *PESC'94 Rec.*, pp. 52–58.

[118] A. G. M. Strollo, "A new SPICE subcircuit model of power PiN diode," *IEEE Trans. Power Electron.*, vol. 9, no. 6, pp. 553–559, 1994.

[119] N. J. Conway and J. G. Lacy, "Integrated reverse-recovery model of the power bipolar diode for SPICE3," *Electron. Lett.*, vol. 29, no. 15, pp. 1392–1394, July 1993.

[120] P. Tounsi, J. M. Dorkel, and P. Leturcq, "Thermal modeling for electrothermal simulation of power devices or circuits," in *5th Europ. Conf. Power Electronics and Applications*, 1993, pp. 155–160.

[121] B. S. Wu and F. A. Lindholm, "One-dimensional nonquasi-static models for arbitrary and heavily doped quasineutral layers in bipolar transistors," *IEEE Trans. Electron Devices*, vol. 35, no. 4, pp. 727–737, 1989.

[122] L. O. Chua and C. C. Chang, "High-speed nonlinear circuit models for p-n junction diodes," *Int. J. Circ. Theory Appl.*, vol. 16, no. 2, pp. 157–190, Apr. 1988.

[123] R. B. Darling, "A full dynamic model for pn-junction diode switching transients," *IEEE Trans. Electron Devices*, vol. 42, no. 5, pp. 969–976, 1995.

[124] Z. Hossain, E. X. Yang, C. L. Ma, V. A. K. Temple, and K. J. Olejniczak, "A physics-based MCT model using the lumped-charge modeling technique," in *PESC'96 Rec.*, pp. 23–28.

[125] P. O. Lauritzen, N. Talwalkar, B. Fatemizadeh, and C. L. Ma, "A power BJT model for circuit simulation," in *PESC'96 Rec.*, pp. 50–55.

[126] I. Budihardjo and P. O. Lauritzen, "The lumped-charge power MOSFET model, including parameter extraction," *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 379–387, 1995.

[127] C. L. Ma, P. O. Lauritzen, and J. Sigg, "A physics-based GTO model for circuit simulation," in *PESC'95 Rec.*, pp. 872–878.

[128] C. L. Ma and P. O. Lauritzen, "A systematic technique to modeling of power semiconductor devices for power electronic simulation," in *Northcon'94 Rec.*, pp. 54–59.

[129] C. L. Ma, P. O. Lauritzen, P.-Y. Lin, I. Budihardjo, and J. Sigg, "A systematic approach to modeling of power semiconductor devices based on charge control principles," in *PESC'94 Rec.*, pp. 31–37.

[130] C. L. Ma, P. O. Lauritzen, P. Turkes, and H. J. Mattausch, "A physically-based SCR model," in *PESC'93 Rec.*, pp. 53–59.

[131] C. L. Ma and P. O. Lauritzen, "A simple power diode model with forward and reverse recovery," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 342–346, 1993.

[132] ——, "A simple power diode model with forward and reverse recovery," in *PESC'91 Rec.*, pp. 411–415.

[133] P. O. Lauritzen and C. L. Ma, "A simple diode model with reverse recovery," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 188–191, 1991.

[134] H. Goebel, "A unified method for modeling semiconductor power devices," *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 497–505, 1994.

[135] H. Goebel, R. Kraus, and H. J. Mattausch, "A hybrid-method for modeling semiconductor power devices," in *PESC'93 Rec.*, pp. 45–52.

[136] H. Goebel and K. Hoffmann, "Full dynamic power diode model including temperature behavior for use in circuit simulators," in *Proc. ISPSD'92*, pp. 130–135.

[137] ——, "Power diode HYBRID model with forward and reverse recovery for use in circuit simulators," in *Proc. APEC'92*, pp. 426–432.

[138] T. Vogler, A. Schloegl, D. Schroeder, and N. Kasahara, "Modeling and characterizing power semiconductors at low temperatures," in *Proc. IPEC-Yokohama'95*, pp. 1237–1243.

[139] T. Vogler, A. Schloegl, and D. Schroeder, "Modeling and characterizing power semiconductors at low temperatures," in *Proc. ISPSD'94*, pp. 237–242.

[140] D. Metzner, T. Vogler, and D. Schroeder, "A modular concept for the circuit simulation of bipolar semiconductors," *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 506–513, 1994.

[141] T. Vogler and D. Schroeder, "A new and accurate circuit-modeling approach for the power diode," in *PESC'92 Rec.*, pp. 870–876.

[142] T. Hsu and L. Vu-Quoc, "A rational formulation of thermal circuit models by finite element method and model reduction techniques for electrothermal simulation," in *1994 IEEE 4th Workshop Computers in Power Electronics*, pp. 67–72.

[143] P. A. Persson, "A circuit simulation model for the high power diode," in *EPE'91 Proc.*, vol. 2, pp. 458–463.

[144] S. Platzek, "Simulation of power electronic circuits and devices" in *Proc. 25th Universities Power Engineering Conf.*, 1990, pp. 57–60.

[145] P. L. B. Teixeira, "Modeling of bipolar power transistors for CAD," in *Europ. Conf. Electronic Design Automation 1981*, pp. 29–33.

[146] Y.-T. Chung, Y.-S. Seo, D.-Y. Sung, Y.-B. Lim, Y.-C. Kim, M.-T. Cho, and S.-K. Kim, "A study on circuit simulation using GTO thyristor modeling," in *Rec. Power Conversion Conf.*, Yokohama, Japan, 1993, pp. 557–562.

[147] J. C. Bowers and H. E. Nienhaus, "Model for high-power SCR's extends range of computer-aided design," *Electronics*, vol. 50, no. 8, pp. 100–105, Apr. 1977.

[148] K. B. Hong and R. C. Jaeger, "Power MOSFET modeling and application at liquid nitrogen temperature," in *Proc. Symp. Low Temperature Electronic Device Operation*, 1991, pp. 238–245.

[149] K. Shenai, G. A. Franz, S. Paul, and S. Haque-Ahmed, "A novel circuit simulation model of large area power MOSFET's suitable for high-frequency power switching applications," in *Tech. Papers 4th Int. High Frequency Power Conversion Conf.*, 1989, pp. 331–356.

[150] Y. Nakagomi and T. Otani, "The third generation IGBT and its model for circuit simulations," in *Proc. PCIM'93 Europe*, pp. 223–227.

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