Abstract
This paper presents a compact model considering the high-frequency and noise effects at the gate of MOS transistors which are caused by the channel resistance in series to the gate capacitance. Real part of input impedance, non-quasistatic charge variations and induced gate noise with correlation to the drain noise are the results. A model equation of the induced gate noise is developed for MOSFETs with very short channel lengths. Comparisons with measurements verify the accuracy of the model and its validity for short and long channel transistors.

Introduction
The continuous reduction of the minimum structures in CMOS technology leads to an enormous improvement of the high-frequency characteristics of MOS transistors and CMOS has now become an interesting candidate for RF applications. However to take full advantage of the transistor performance and to optimize the circuit design adequate device models for circuit simulations are absolutely necessary. A lot of work has been done during the last years to improve MOSFET models by considering high-frequency effects and describing noise characteristics (1,2,3). The MOS models of standard circuit simulators did not take into account the gate noise and its correlation to the drain noise despite the existing (long channel) model equation by van der Ziel (4). It was a widespread opinion that the contribution of this noise source could be neglected. However this assumption is not correct e.g. in the case of LNA (low noise amplifier) design and optimization (5). Furthermore recent measurements have shown that the gate noise of deep-submicron MOSFETs can be up to a factor 30 higher than predicted by van der Ziels model (6).

The MOSFET model BSIM4 now includes a description of the gate noise (7) but the method of implementation does not allow a correct reproduction of the correlation between gate and drain noise.

The purpose of this work is to develop a gate noise model which can accurately predict the noise even of extreme short channel transistors and to show an implementation in the circuit simulator which provides correct results of the main high-frequency effects and the noise characteristics inclusive the gate-drain noise correlation.

Equations for Drain and Gate Noise
The channel of the MOS transistor is divided into a gradual channel region (I) and a velocity saturation region (II) (see fig. 1); the contributions of these regions to the thermal noise are calculated separately. The hot carrier effect is included using an electric-field-dependent electron temperature. For the drain current noise the model derivation has been presented in the paper (3); the result is in a slightly modified form:

\[ i_{nd}^2 = i_{nd}^2 + i_{nd}^2 = 4kT \left( g_{nd} + g_{nd} \right) \Delta f \] (1)

with

\[ g_{nd} = \frac{\mu Q_{inv}}{L^2} + \frac{i_d}{E_s L} \left( \beta V_{ds} - V_{dsat} \right) \] (2)

\[ g_{nd} = \frac{i_d}{E_s L} \beta V_{ds} - V_{dsat} \] (3)

The short-channel effects are considered with \( Q_{inv} \), the total inversion layer charge. The terms with the parameter \( \beta \) describe the influence of increasing electron temperature at high fields in very short transistors.

The induced gate noise current caused by voltage fluctuations in the channel can be written in the form:

\[ i_{ng}^2 = \omega \left( C_i V_{ng} + C_\mu V_{ng} \right)^2 \] (4)

with

Fig.1: Cross-section of the MOSFET
\( C_I = WL C_{ox} = \frac{L}{L} C_t \) \hspace{1cm} \( C_{II} = W \Delta L C_{ox} = \frac{\Delta L}{L} C_t \) 

\( v_{ngI} \) and \( v_{ngII} \) are the averaged voltage variations in region I and II respectively:

\[ v_{ngI} = \frac{1}{L} \int \Delta v(x) dx \] \hspace{1cm} \[ v_{ngII} = \frac{1}{\Delta L} \int \Delta v(x) dx \]

An explicit calculation of \( v_{ngI} \) and \( v_{ngII} \) including all short channel effects and variable electron temperature is very tedious and leads to a complicated result. A model intended for circuit simulations, however, should be compact and as simple as possible. Therefore an approximation is used which is obtained by the assumption that the averaged noise voltages in the channel are proportional to the amount of drain current noise, since both noises have the same origin (but this does not mean that full correlation is assumed):

\[ v_{ngI} = r_I \sqrt{(a_{n1} i_{nd})^2 + (a_{n2} i_{ndI})^2} \] \hspace{1cm} \[ v_{ngII} = r_{II} \sqrt{(a_{n1} i_{nd})^2 + (a_{n2} i_{ndII})^2} \]

\( r_I \) and \( r_{II} \) are effective channel resistances which together with the constant parameters \( a_{n1} \) and \( a_{n2} \) give the relation between noise voltage and noise current.

\[ r_I = r_{gs} + r_s \] \hspace{1cm} \[ r_{II} = r_{gs} + r_s + r_{sat} \]

\( r_{gs} \) is the gate-channel resistance determining the non-quasistatic charging of the transistor channel; it is proportional to the inverse of the transconductance \( g_m \). \( r_s \) is the voltage-dependent source resistance and \( r_{sat} \) is the resistance of the velocity saturation region.

\[ r_{gs} = \frac{a}{g_m} \] \hspace{1cm} \[ r_{sat} = \frac{1}{W c_{ox} v_{sat}} \]

Introducing two noise resistances \( r_{ngI} \) and \( r_{ngII} \) which are obtained from the above equations:

\[ r_{ngI} = \left( \frac{L}{L} r_I + \frac{\Delta L}{L} r_{gl} \right) a_{n1}^2 g_{stI} \] \hspace{1cm} \[ r_{ngII} = \left( \frac{L}{L} r_I + \frac{\Delta L}{L} r_{gl} \right) a_{n2}^2 g_{stII} \]

the induced gate noise current can be expressed by:

\[ i_{ng}^2 = \omega^2 C_s^2 4kT \left( r_{ngI} + r_{ngII} \right) \Delta f \] \hspace{1cm} \[ i_{ng}^2 = \omega^2 C_s^2 4kT \left( r_{ngI} + r_{ngII} \right) \Delta f \]

For long-channel transistors \( \Delta L/L \) and \( g_{stII} \) are approximate-ly zero and (in saturation) \( g_{stI} \) is proportional to \( g_m \). The new equations of thermal drain and gate noise reduce then to the classical noise equations (van der Ziel (4)). The parameter \( a_{n1} \) is therefore determined by the gate noise of long-channel transistors, whereas \( a_{n2} \) is used to adjust the model to the noise characteristics of short-channel devices.

Fig. 2: Equivalent circuit of the model

**Model Implementation in Circuit Simulator**

Fig. 2 shows an equivalent circuit representing the model of drain current noise, induced gate noise, and the correlation between them; it also contains the main elements which are necessary for modeling the high–frequency behavior of the MOSFET (the extrinsic resistors at gate, drain and source and the resistive network at the bulk are not shown). This model representation has the advantage that it can be added to the external nodes of any existing MOSFET model (e.g. BSIM) without changes of the topology or the equations of that model. The model can be implemented as a subcircuit (e.g. in PSpice) or directly by mathematical functions in the programming language.

The functions for the current sources \( i_{go} \) and \( i_c \) and their small-signal results are:

\[ i_{go} = \frac{d}{dt} (Q_{gs}) = j \omega C_{gs} v_{gs} \] \hspace{1cm} \[ i_c = \frac{d}{dt} (C_{gs} v_{gs}) = j \omega C_{gs} v_{gs} \]

The voltage \( v_{rs} \) consists of the voltage drop across the (noiseless) resistor \( r_{geff} \) and the noise voltages \( v_{ngu} \) and \( v_{ngc} \). The noise voltages and the contribution from \( i_{go} \) are uncorrelated; but in the following equations only the superposition of \( v_{ngu} \) and \( v_{ngc} \) is shown correctly and the component of \( i_{go} \) is just added for the sake of simplicity and clarity. Then for \( i_c \) one gets:

\[ i_c = \frac{j \omega (r_{geff} C_{gs} i_{go} + C_{gs} \sqrt{v_{ngu}^2 + v_{ngc}^2})}{1 + j \omega r_{geff} C_{gs}} \]

Since \( i_{go} \) is the gate current (resulting from \( C_{gs} \)) of the standard MOSFET model the obtained gate current \( i_g \) is now:
\[ i_s = i_{gs} - i_e = \frac{i_{gs} - j\omega C_s \sqrt{v_{ngu}^2 + v_{ngc}^2}}{1 + j\omega r_{geff} C_s} = \frac{i_{gs} + i_{ng}}{1 + j\omega r_{geff} C_s} \] (21)

This solution is equal to the result which is obtained by the series-connection of the gate-source capacitance and a channel resistance (8), since \( r_{geff} \) is given by:

\[ r_{geff} = r_g \frac{C_{gs}}{C_s} \] (22)

Due to the channel resistance the channel charge cannot immediately respond to changes of the applied transistor voltages; the non-quasistatic behavior is therefore modelled with it. Furthermore the real part of the transistors input impedance is not only equal to the gate resistance; the channel resistance is a not neglectable, in RF-transistors with finger structures even dominant part of it.

The induced gate noise \( i_{ng} \) is determined by the two voltage sources \( v_{ngu} \) and \( v_{ngc} \). \( v_{ngu} \) is a noise source describing the uncorrelated part of the gate noise. According to equ. (17) the function for \( v_{ngu} \) is:

\[ v_{ngu} = (1-c^2)4kT(r_{ngl} + r_{ngl}) \] (23)

\( v_{ngc} \) however is a voltage-controlled voltage source, since its purpose is to get the correlation to the noise source \( i_{nd} \) which is determined by equ. (1). The control voltage is the voltage drop \( v_{ns} \) across the correlation resistance \( r_{nc} \).

\[ v_{ngc} = c v_{ns} = c r_{nc} i_{nd} \] (24)

\[ r_{nc} = \sqrt{r_{ngl} + r_{ngl}} \] (25)

For the correlation coefficient \( c \) a constant value is used. (\( c \) has a real value since the imaginary correlation of \( i_{ng} \) to \( i_{nd} \) is obtained by the multiplication of the noise voltage with \( j\omega C_s \).

**Results**

The four noise parameters of the MOSFET (drain current noise, gate noise, and complex correlation coefficient) have been extracted from noise measurements with the help of a strategy described in (6). Fig. 3 shows a comparison of the measured and simulated drain current noise of NMOS transistors with 0.25 \( \mu m \) and 1.05 \( \mu m \).

The measured and simulated induced gate noise of the 0.25 \( \mu m \) transistor is shown in fig. 4. The result of the classical long channel model is also included in this figure. It demonstrates that the values of the old model can be up to a factor 30 too small whereas the new model reproduces the measured values very well.

The dependence of the gate noise on the channel length is plotted in fig. 5 to demonstrate the scalability of the model. Additionally it is shown how the noise origins in the two transistor regions contribute to the total gate noise. In long channel transistors region II is neglectable, with decreasing \( L \) however this part becomes more and more important. Below \( L=0.35 \mu m \) a reduction of \( L \) (and therefore the area of the gate capacitance) does not lead to a further reduction of the gate noise but to an increase of it.
Conclusion

The channel resistance of MOSFETs determines not only the voltage dependence of the drain current and the drain current noise, it also causes a real part of the input impedance, a non-quasistatic behavior of the channel charge and an induced gate noise. This paper has shown how these effects can be incorporated in any MOSFET model for circuit simulation. The correlation between drain and gate noise is also considered correctly. The model equation for the induced gate noise has been obtained by a simple but physically reasonable approach which provides very satisfactory results. The voltage dependence and the influence of the channel length are accurately reproduced by the models of drain and gate noise; this has been verified by comparisons with extracted data from RF noise measurements.

The consideration of the modelled effects is essential for correct simulations of many RF applications, e.g. in the case of input matching and noise optimization.

References

(7) J.S. Goo et al., “The equivalence of van der Ziel and BSIM4 models in modeling the induced gate noise of MOSFETs”, *IEDM* 2000, pp. 811-814