Thermal Channel Noise of Quarter and Sub-Quarter Micron NMOS FET's

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ABSTRACT

We present a simple and efficient method for the extraction of thermal channel noise of MOS FET's in quarter and sub-quarter micron technologies from NF50 (noise figure at 50 Ohm source resistance) measurements. For shorter channel lengths the experimental results shows a continuously rising deviation from the classical long channel theory [1]. For a 0.18 µm technology a $\gamma \approx 6$ instead of 2/3 in saturation was extracted (increase of factor 9 compared to the long channel theory).

INTRODUCTION

Due to continuous reduction of minimum channel length in CMOS technologies in the last years, CMOS has become a candidate for RF applications. For quarter and sub-quarter micron technologies transit frequencies (f_t) in the range of 40-70 GHz and maximum oscillation frequencies up to 40 GHz and more are possible for NMOS transistors [2]. For these devices the classical assumption of thermal equilibrium in the calculation of the channel noise is questionable. Additional, so called hot carrier noise is observed for short channel transistors [3-6].
But until now only results for ≈0.8µm [3] or 0.5µm [4] technologies are available. In our paper for the first time results for quarter and sub-quarter micron technologies are presented. The reliability of this method is verified by comparing results from DC measurements (g_{d0} model) with results from RF noise measurements for almost ideal long channel transistors (1.05µm).
In conclusion, the purpose of this work is to introduce an efficient extraction method for thermal channel noise of extreme short channel transistors and secondly to give necessary hints for RF–CMOS design, where finding the optimum between noise performance and AC performance is one of the key issues (e.g. LNA's, which are an essential part of system on a chip solutions for wireless communication).

MEASUREMENTS, TEST STRUCTURES AND DE-EMBEDDING

A commercial noise figure measurement set up was used (ATN) and on wafer measurements from 600 MHz up to 6 GHz have been performed. This frequency range is high enough to clearly separate 1/f and white noise of our test structures (Tab.1). These test structures are optimized for RF applications (folded finger structures). The noise measurements are de-embedded with the noise de-embedding method presented in [7]. Exact de-embedding of the noise measurements is very important, because the influence of the parasitics (pads and substrate resistors) on the NF50 value can be significant [8]. At the same structures also S-parameters are measured and de-embedded with the usual standard method.

EXTRACTION METHOD

For the exact extraction of the thermal noise all additional noise sources in the small signal equivalent circuit have to be considered. It is not necessary to have an exact small signal equivalent circuit of the transistor, because the measured S- or y-parameters are used directly for the calculations. The circuits in Fig.1 and Fig.2 are used to calculate the contributions of the noise sources to the NF50 value where Fig.1 is only used for the calculation of the parasitics and R_{50} contribution and Fig.2 is used for the calculation of the channel noise contribution. The gate resistance is extracted from the layout and the source and drain resistors are extracted from DC measurements. For these two resistors a gate voltage dependence is taken into account [9]. The substrate resistor and the junction substrate capacitor are extracted from the two port parameter z22. The NF50 value of the whole circuit is calculated using (1). In this equation all values are known except the contribution of the channel noise $\left(\overline{i^2_{out}}\right)_{id}$.

$$NF50 = \frac{\left(\overline{i^2_{out}}\right)_{R50} + \left(\overline{i^2_{out}}\right)_{Rg} + \left(\overline{i^2_{out}}\right)_{Rs} + \left(\overline{i^2_{out}}\right)_{Rd} + \left(\overline{i^2_{out}}\right)_{Rsub} + \left(\overline{i^2_{out}}\right)_{id}}{\left(\overline{i^2_{out}}\right)_{R50}} \qquad (1)$$

With the help of Fig.2 and (1) the channel noise $\overline{i_d^2}$ is calculated. In Fig.3 the extracted channel noise is plotted for two different bias points versus frequency. To make sure, the gate induced noise is neglectable for all test structures, only frequencies up to 2 GHz ($\lesssim f_t/10$) are taken into account for the calculation of the mean value for each bias point.

RESULTS AND DISCUSSION

The expected thermal channel noise for long channel transistors with the assumption of thermodynamic equilibrium is [1],

$$\frac{\overline{i_d^2}}{\Delta f} = \gamma 4 k_B T g_{d0} \quad \text{with } \gamma = \begin{cases} 1 & \text{linear region} \\ \approx 2/3 & \text{saturation region} \end{cases} \quad (2)$$

where g_{d0} is the channel conductance at $V_{ds}=0$.
For $V_{ds}\neq 0$ the mobility reduction caused by the lateral electric field must be considered in (2) yielding,

$$\frac{\overline{i_d^2}}{\Delta f} = \gamma 4 k_B T g_{d0} \frac{\mu_{eff}}{\mu_{eff}\big|_{Vds=0V}} \quad (3) \qquad \mu_{eff} = \frac{\mu_s}{\left(1+\left(\frac{E_X}{E_{sat}}\right)^{\beta}\right)^{\frac{1}{\beta}}} \quad (4)$$

with E_X being the lateral electric field (for the sake of simplicity: E_X=Vds/L in linear region and E_X=(Vgs-Vth)/L in saturation region) and $E_{sat}=v_{sat}/\mu_s$. For μ_s the mobility model (mobmod=1) of the BISIM3v3 SPICE model is used [10]. The model parameters for this mobility model together with β (≈2 [11]) and v_{sat} have been extracted from the DC measurements. Fig.4-5 show the extracted channel noise versus Vgs for two different channel lengths (1.05 µm and 0.25µm) in linear region and in saturation region for the 0.25 µm technology. The difference between the extracted noise values and the g_{d0} model (3) is relatively small for the long channel transistor but much more pronounced for the short channel transistor, especially in saturation.
Similar plots for 0.25 µm and 0.18 µm channel lengths are shown for the 0.18 µm technology (Fig.6-7). For these devices the differences between extracted noise and g_{d0} model are enormous.
In Fig. 8 the extracted γ values for different channel lengths versus Vds for the 0.25 µm technology are plotted. The reduction of γ from ≈ 1 in linear region to ≈ 2/3 in saturation can be seen for transistor 4. For smaller channel lengths the thermal equilibrium noise is superimposed by hot carrier effects which rise with the Vds voltage, also increasing γ up to values of 2.5.
The same plot is also shown for the 0.18 µm technology (Fig.9) where γ even rises up to a value of ≈ 6 in saturation. In Fig.10 γ for different channel lengths and for both technologies is plotted in saturation. The increase of γ with channel length reduction is moderate up to a channel length of ≈ 0.30 µm. Below this value, the increase of γ is extreme.

PHYSICAL INTERPRETATION

According to [1], the thermal noise spectral density including hot electron effects is given by

$$\frac{\overline{i_d^2}}{\Delta f} = \frac{4 k_B T}{L^2 I_d} \int_0^{V_d} \frac{T_e}{T} g^2(V) dV \quad (5)$$

where T is the lattice temperature, T_e is the electron temperature, g(V) is the channel conductance at any given point along the channel, I_d is the drain current and L is the channel length. Fig.11 gives the relation between the electron temperature and the electrical field [12] and in [13] an analytical relation between electron temperature and electrical field is published,

$$T_e = T + \frac{2}{3k_B} q \bar{v} \tau_e E \quad (6)$$

where $\bar{v}$ is the average drift velocity, E is the electrical field and τ_e is the energy relaxation time. In Fig.11 it is shown, that the averaged equivalent electron temperature for short channel transistors is in the range of a few thousand Kelvin.

CONCLUSION

The increase of the factor γ with smaller channel length is only moderate up to ≈ 0.30 µm. Further channel length reduction increases γ up to a factor 9 compared to classical long channel theory. To find the optimum between the AC performance and noise performance, the precise knowledge of the noise increase with channel length reduction plays a key role for low noise RF-design.

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Tab.1: Characterized transistor geometries (designed values)

No.	0.25 µm Technology	0.18 µm Technology
1	96µm/0.25µm	108µm/0.18µm
2	96µm/0.35µm	108µm/0.21µm
3	96µm/0.50µm	108µm/0.25µm
4	96µm/1.05µm	108µm/0.30µm

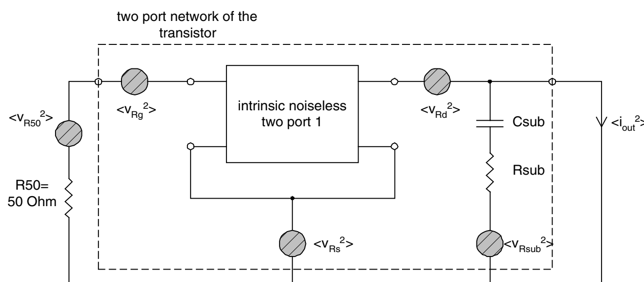

Fig.1: Circuit for the calculation of the contribution of gate resistance ($<v_{rg}^2>$), source resistance ($<v_{Rs}^2>$), drain resistance ($<v_{Rd}^2>$), substrate resistance ($<v_{Rsub}^2>$) and the 50 Ohm resistance ($<v_{R50}^2>$) to the NF50 value. The intrinsic noiseless two port represents the whole transistor except the substrate components (separated with y parameter subtraction).

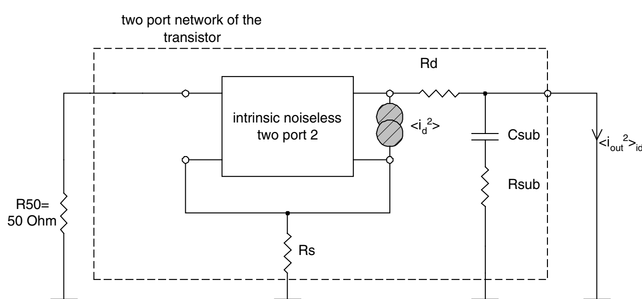

Fig.2: Circuit for the calculation of the contribution of the channel noise ($<i_d^2>$) to the NF50 value. The intrinsic noiseless two port represents the whole transistor except the substrate components (separated with y parameter subtraction) and drain (R_d) and source (R_s) resistores. (separated with z parameter subtraction).

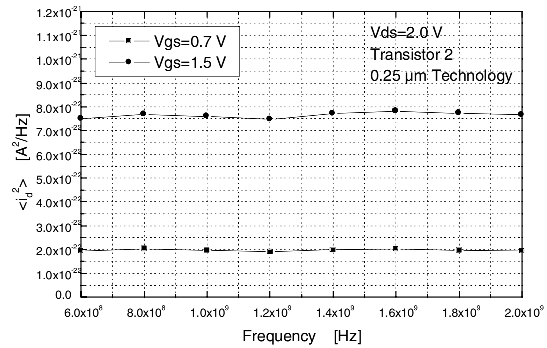

Fig.3: Extracted channel thermal noise versus frequency for two different operating points of transistor 2 of the 0.25 µm technology.

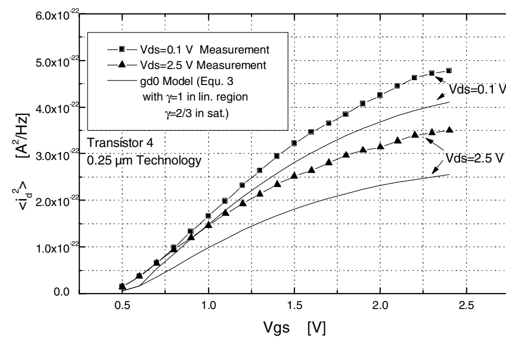

Fig.4: Thermal channel noise of the $4.2{*}L_{min}$ transistor (No.4) of the 0.25 µm technology versus Vgs in linear (Vds=0.1V) and saturation (Vds=2.5V) region.

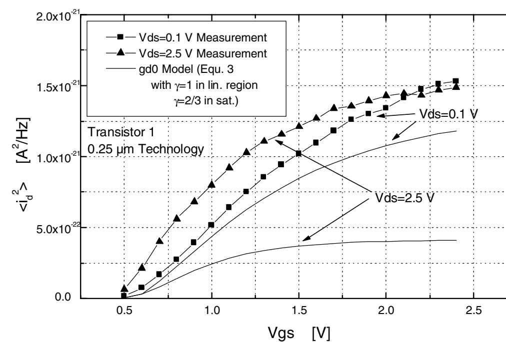

Fig.5: Thermal channel noise of the L_{min} transistor (No.1) of the 0.25 µm technology versus Vgs in linear (Vds=0.1V) and saturation Vds=2.5V) region.

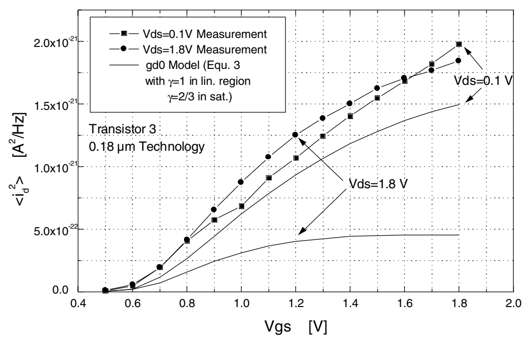

Fig.6: Thermal channel noise of the 1.4*L_{min} transistor (No.3) of the 0.18 µm technology versus Vgs in linear (Vds=0.1V) and saturation (Vds=1.8V) region.

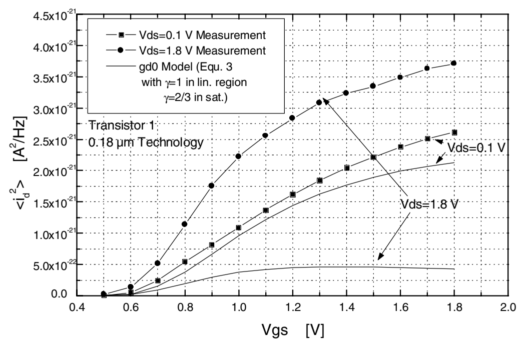

Fig.7: Thermal channel noise of the L_{min} transistor (No.1) of the 0.18 µm technology versus Vgs in linear (Vds=0.1V) and saturation (Vds=1.8V) region.

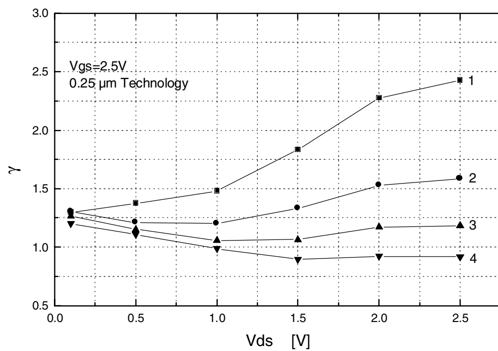

Fig.8: Calculated γ factors in saturation (see Equ. (3)) for different channel lengths (transistor 1-4) of the 0.25 µm technology versus Vds.

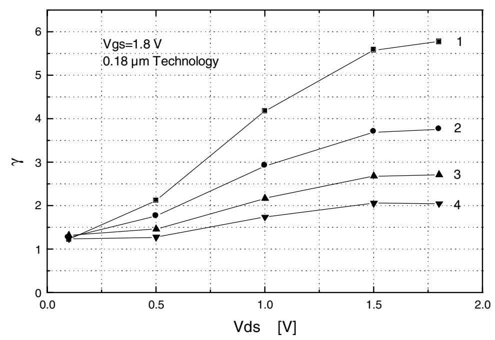

Fig.9: Calculated γ factors in saturation (see Equ. (3)) for different channel lengths (transistor 1-4) of the 0.18 µm technology versus Vds.

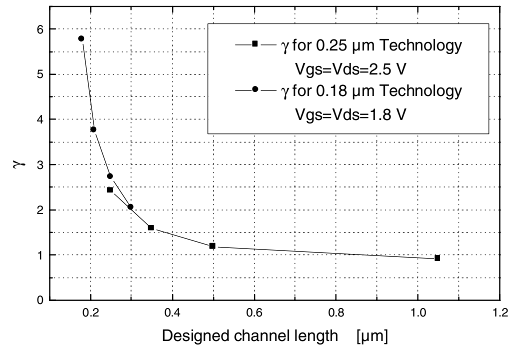

Fig.10: Calculated γ factors (see Equ. (3)) versus channel length for transistor 1-4 in saturation for the 0.18 and 0.25 µm technology.

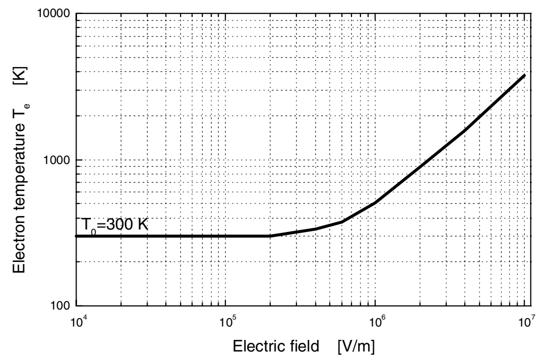

Fig.11: Equivalent electron temperature versus electrical field [12]