A New Mobility Model for Pocket Implanted Quarter Micron n-MOSFETs and Below

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ABSTRACT
A new, analytical, physical-based effective surface mobility model valid in all regimes of device operation from weak to strong inversion is introduced. The model accounts for all relevant scattering processes vs. the electric field and temperature as well as for the lateral non-uniform 2-D doping profile in pocket implanted MOSFETs. Measurements show that the mobility degradation due to Coulomb scattering with ionized dopants in the heavily doped pocket implanted regions cause a reduction of the surface mobility of up to 30% at low gate-to-source overdrive voltage ($V_{GS} = V_{th} + 100...200\text{mV}$).

I. INTRODUCTION
With the downsizing of CMOS devices the supply voltage must be scaled down as well as the threshold voltage. Last one however cannot be scaled in proportion to the supply voltage because it is limited by the subthreshold current behavior.
In order to reduce the leakage current of devices with minimum channel length\(^1\) and to increase the saturation current (and with it the performance) of the nominal devices at the same time, pocket implants as sketched in fig. 1 are generally used.

![Fig. 1: Lateral channel doping profile of pocket implanted MOSFETs (0.25µm) obtained from process simulation.](image)

Pocket implants retard the short channel effect thus the decrease of threshold voltage of very short devices (fig.2). It could be shown that with an optimized pocket implant process the saturation current is up to 10% higher compared to a conventional optimized junction technology without increasing the leakage current of the minimum devices.

![Fig. 2: Measured threshold voltage ($V_{th} @ V_{DS}=50\text{mV}$) vs. the designed length with and without pocket implant. Devices without pocket implants show only a slight reverse short channel effect (due to lateral interstitial diffusion) while pocket implanted MOSFETs show a strong increase of $V_{th}$ with decreasing channel length.](image)

The use of pocket implants causes a strong non-uniform lateral doping profile and with it a pronounced increase of the average channel doping $N_{CHeff}$ with decreasing design length $L_{des}$ as shown in fig.3.

![Fig. 3: Averaged doping $N_{CHeff}$ of pocket implanted MOSFETs vs. the designed length. $N_{CHeff}$ is obtained by integrating $N_C(x)$ (fig.1) near the surface Si/SiO$_2$ along the channel between the pn-junctions divide by $L_{CH}$.](image)

\(^1\)minimum channel length = (nominal channel length - 3 sigma of the channel length variation)
Caused by this increase the effective mobility \( \mu_{\text{eff}} \) is more and more degraded due to Coulomb scattering with ionized dopants at low vertical electrical fields (low \( V_{DS} \)). In most circuit models [1-3] simple mobility models [4, 5] are used to describe the effective surface mobility neither accounting for the degradation by Coulomb scattering in heavily doped MOSFET’s (only the so called ‘universal curve’ [6] is modeled) nor accounting for the lateral non-uniform doping profile. This neglect can cause simulation errors in the transconductance of short n-MOS pocket implanted devices of up to 50% which can not be tolerated in today’s circuit simulations.

Therefore purpose of the work is to develop a mobility model for compact MOSFET modeling which describes \( \mu_{\text{eff}} \) as function of the electric field and temperature as well as of the averaged channel doping for each designed length.

### II. MOBILITY MODEL

The three most relevant scattering processes in MOSFET devices are the (screened) Coulomb scattering \( \mu_{C} \), the phonon scattering \( \mu_{ph} \) and the surface roughness scattering \( \mu_{sr} \). The single mobility components are combined with the simple Mathiessen-rule resulting in

\[
\mu_{\text{eff}} = \left( \mu_{C}^{-1} + \mu_{ph}^{-1} + \mu_{sr}^{-1} \right)^{-1}
\]

where \( \mu_{\text{eff}} \) is the effective surface mobility at low drain-source voltage \( V_{DS} \) (negligible lateral electrical field, no velocity saturation effect [4]).

#### A. Coulomb scattering \( \mu_{C} \)

A formula for the Coulomb limited mobility is given in [6] by S. Villa et al.

\[
\mu_{C} = \mu_{0} \frac{L_{s}}{N_{CH} L_{CH}} \left( 1 + \frac{L_{CH}}{L_{s}} \right)^{2}.
\]

\( L_{s} = (L_{CH}^{2} + L_{EF}^{2})^{1/2} \) is the effective screening length with \( L_{EF} = \frac{\pi \hbar^{2} q^{3/2} m^{*}}{e^{2}} \) being the Thomas-Fermi value, \( L_{CH} = 2.5 \text{nm}(300 \text{K}/T)^{1/2} \) is the thermal length of the carriers with \( T \) being the temperature, \( L_{CH} = \frac{2\pi}{kT} q \sqrt{Q \cdot \alpha_{B}} \) is the Debye-Hückel value with the inversion charge density \( Q \cdot \alpha_{B} \) and \( N_{CH} \) is the averaged channel doping concentration (fig. 3) and \( \mu_{0} \) is a parameter. To hold (2) simple and analytical solvable \( \varepsilon \) is simply set to the dielectric constant of silicon \( \varepsilon_{Si} \) contrary to [6].

#### B. Phonon scattering \( \mu_{ph} \)

Gamiz et al. [7] have shown that the phonon limited mobility may be approximated by

\[
\mu_{ph}|_{T=300K} = \frac{\mu_{B}}{1 + (E_{ph} / E_{0})^{\alpha}}
\]

at room temperature, where \( \mu_{B} = 0.147 \text{ m}^{2}/\text{Vs} \) is the phonon limited bulk mobility and \( E_{0} = 7 \times 10^{3} \text{ V/m} \) is a constant. \( E_{ph} \) is the effective electric field which is generally defined as

\[
E_{ph} = \frac{1}{\varepsilon_{Si}} \left( Q_{s} + \eta \cdot Q_{i} \right) \quad \text{at} \ V_{DS} = 0V
\]

\[
\Rightarrow E_{ph} (\text{NOMOS}) = \frac{C_{CH}}{\varepsilon_{Si}} \left( \frac{1}{2} V_{GS} + (V_{TH} - V_{FB} - 2 \delta_{T}) \right)
\]

where \( Q_{s} \) and \( Q_{i} \) are the depletion and inversion charge densities and \( \eta = 1/2 \) for NMOS and \( \eta = 1/3 \) for PMOS transistors respectively [8]. \( V_{GS} \) is the effective gate-source overdrive voltage (compare appendix). The temperature influence is taken into account by multiplying the factor \((T/300K)^{\alpha}\) with \( \alpha = 2.4 \) giving

\[
\mu_{ph} = \frac{\mu_{ph}|_{T=300K}}{(T/300K)^{\alpha}}
\]

#### C. Surface roughness scattering \( \mu_{sr} \)

Since the Si/SiO\(_{2}\) interface is not ideally flat the carriers are scattered by this potential fluctuations at high electrical fields. According to [9,10] the surface roughness mobility is inversely proportional to the square of the effective electrical field \( E_{eff} \)

\[
\mu_{sr} = \frac{\delta}{E_{eff}^{2}}
\]

where \( \delta \) is a fitting parameter depending on the quality of the Si/SiO\(_{2}\) interface. Since the temperature dependence of this scattering process is very low [6] and to keep the circuit mobility model simple (only one temperature parameter \( \alpha \) in (5) is used) the temperature coefficient of \( \mu_{sr} \) is neglected in this work.

### III. RESULTS AND DISCUSSION

To prove the developed analytical mobility model (1) measurements have been performed on MOSFET’s of a quarter micron CMOS process.

Taking the drift and diffusion component of the channel current into account the measured large signal output resistance \( R_{m} \) of long and short channel transistors at a low drain-source voltage \( V_{DS} = 10...50\text{mV} \) is described by (7) (compare appendix)

\[
R_{m} = \frac{L_{CH} \mu_{eff} C_{CH} (V_{GS} - F_{B} \frac{V_{DS}}{2} - \phi_{i})}{W \mu_{eff} L_{CH} C_{CH} (V_{GS} - F_{B} \frac{V_{DS}}{2} - \phi_{i}) + R_{S} + R_{D}}
\]

where \( L_{CH} \) is the channel length, \( F_{B} \) is a correction factor for the linearized bulk charge \[11\], \( \phi_{i} \) is the thermal voltage and \( R_{S} \) and \( R_{D} \) are the source and drain series resistances. The mobility at a designed (drawn) length \( L_{des} \) and an overdrive voltage \( V_{GS} \) can be extracted from the difference of the measured output.
resistance at this bias point of two transistors with the same width but a slightly shorter and larger designed length $W/L_1$ and $W/L_2$

$$\mu_{eff}\big|_{L_{ds}} = \frac{L_2 - L_1}{W_{C'OX} \left(V_{GS_{eff}} - F_B \left(\frac{V_{ds}}{2} - \phi_2\right) \right)} \left(R_{\infty\infty} - R_{\infty\infty}'\infty\infty\right)$$

where $L_1 = L_{ds} - \Delta L$ and $L_2 = L_{ds} + \Delta L$.

The advantage of this procedure (8) is that $L_{C'OX}$, $R_3$ and $R_p$ are not necessary to be known, which are in general critical to be extracted correctly in quarter micron technologies and below. Furthermore due $V_{DS} / 2 \phi_2 \approx 0$V (for $V_{GS} = 50mV$ and room temperature) the value of the fitting parameter $F_B$ plays no role during the extraction of $\mu_{eff}$ (from optimization routines $F_B$ was fitted to a constant value of 1.1 for all channel length, operating points and process variations (pocket and not pocket implanted FETs)). With (8) the effective mobility $\mu_{eff}$ of devices with $L_{des} = 5, 2, 1, 0.8, 0.5, 0.25 \mu m (W = 10 \mu m)$ has been extracted vs. $V_{GS_{eff}} + 2 V_{TH}$ (for $V_{GS}$, compare (4)) as shown in fig. 4.

![Fig. 4: Effective mobility versus $V_{GS_{eff}} + 2V_{TH}$ (~$E_{off}$ compare (4)) for pocket implanted devices and different designed length at $V_{GS}=50mV$. (Symbols) experimental results, (-----) new model (1), (- - -) BSIM3v3 model $MOBMOD=1$.](image)

The agreement between simulation and experimental data is sufficient taking the new mobility model with the parameters $\mu_0 = 3.75 \times 10^{11} \text{ V/s}, \delta = 4.9 \times 10^{13} \text{ V/s}, \alpha=2.4$ and $N_{C'eff}$ as shown in fig. 3. Even the degradation at low fields and high averaged channel doping (curve $L_{des} = 0.25 \mu m$) due to Coulomb scattering can exactly be modeled. This is decisive for low voltage (power) circuit design. The dotted curve in fig. 4 shows the mobility model characteristic of the BSIM3v3 CMOS circuit model ($MOBMOD = 1$) [3]. While the BSIM3v3 mobility model fits the long channel case good enough, the discrepancy between measurement and simulation of short channel transistors and low $V_{GS}$ is not acceptable.

Fig. 5 shows the influence of pocket implants on the surface mobility. Long and short channel transistors with and without pocket implants are compared. While the mobility for long channel transistors is nearly the same the situation for short channel devices (here $0.5 \mu m$) is quite different. The strong reduction of the mobility of pocket implanted short channel transistors in the Coulomb scattering (partly phonon scattering) dominant region is mainly caused by the increased averaged impurity-concentration.

![Fig. 5: Effective mobility for different designed length with and without pocket implants at $V_{GS}=50mV$. (Symbols) experimental results, (-----) new model (1), (- - -) BSIM3v3 model $MOBMOD=1$.](image)

A comparison of the temperature behavior of the new model (1) and the well known model of [3] is shown in fig. 6. It can be seen that (1) gives excellent agreement to the data.

![Fig. 6: Effective mobility ($V_{GS}=50mV$) for pocket implanted devices, different designed length and temperatures. (Symbols) experimental results, (-----) new model (1), (- - -) BSIM3v3 model $MOBMOD=1$.](image)

Fig. 7 and 8 finally demonstrate results on device transfer $I(V)$ and transconductance $g_m(V)$ characteristics of the pocket implanted devices. In fig. 9 the new mobility model was tested for high values of the drain voltage. It is obvious that an improved mobility model like (1) must be included in standard MOSFET models e.g. [3]
to ensure future low power/low voltage circuit simulations.

Fig. 7: Transfer characteristic of a pocket implanted n-MOSFET (W/L=10μm/5μm) at VDS=0.1V. (Symbols) experimental results, (——) new model (1), (- - -) BSIM3v3 model MOBMOD=1.

Fig. 8: Transfer characteristic of a pocket implanted n-MOSFET (W/L=10μm/0.25μm) at VDS=0.1V. (Symbols) experimental results, (——) new model (1), (- - -) BSIM3v3 model MOBMOD=1.

Fig. 9: Output characteristic of a pocket implanted n-MOSFET (W/L=10μm/0.25μm). (Symbols) experimental results, (——) new model (1).

IV. APPENDIX

The total channel current I_DS consists of a drift and a diffusion component

\[ I_{DS} = I_{d0} + I_{diff} \]

\[ I_{d0} = \frac{W}{L_{CH}} \mu_{eff} C_{ox} \left( V_{GSeff} - \frac{F_m}{2} (\psi_{SL} - \psi_{SO}) \right) \psi_{SL} - \psi_{SO} \]

\[ I_{diff} = \frac{W}{L_{CH}} \mu_{eff} C_{ox} F_m \phi_i \left( \psi_{SL} - \psi_{SO} \right) \]

where \( \psi_{SL} \) and \( \psi_{SO} \) are the surface potentials at drain and source [1, 4]. In the triode region \( (\psi_{ds} - \psi_{SO}) = V_{DS} \).

From (A1) the large signal output resistance \( R_{DS} \) can be defined as

\[ R_{DS} = \frac{\left| \frac{\partial V_{DS}}{\partial I_{DS}} \right|}{I_{DS}} \]

at low \( V_{DS} \) can be derived. The measured output resistance \( R_m = R_{DS} + R_s + R_d \) is the sum of \( R_{DS} \) and the series resistances of source and drain \( R_s \) and \( R_d \).

With the charge sheet approximation the effective gate source voltage \( V_{GSeff} \) at zero back bias \( (V_{SB}=0) \) can be defined as

\[ V_{GSeff} = V_{GS} - V_{FB} + \psi_{SO} + f_c \gamma \sqrt{\psi_{SO}} \]

with \( V_{FB} \) being the flat band voltage and \( f_c \) being the adjusted body effect coefficient to model all short and narrow channel effects with influence on the threshold voltage \([1,11]\).

REFERENCES