AN ANALYTICAL SOURCE-AND-DRAIN SERIES RESISTANCE MODEL OF QUARTER MICRON MOSFETS AND ITS INFLUENCE ON CIRCUIT SIMULATION

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ABSTRACT

An analytical model to describe the bias dependent series resistances R_S and R_D of LDD MOSFETs down to quarter micron and below is introduced. Comparing measurement and simulation results of CMOS ring oscillators it has been found that for low voltage applications ($V_{dd}=1\,\mathrm{V}$) an incorrect description of R_S and R_D can cause a simulation error of up to 30 % in the delay time of CMOS inverters.

1. INTRODUCTION

With the down-scaling of CMOS-devices the accurate modeling of the device parasitics as e.g. the source-and-drain series resistances R_S and R_D (fig. 1) becomes more and more significant. While the device speed itself increases approximately with $(1/l_{ch})^2$ we found that the circuit speed using a quarter micron technology rises nearly with $(1/l_{ch})^{1.4}$ due to parasitic resistances and capacitances [4]. Much emphasis has been placed on modeling the MOS transistor for circuit application. Contrary to this, most hitherto developed models describe the interconnect resistances independent [6, 7] or linear dependent [5] on gate voltage only. This approximation for R_S and R_D is in general sufficient for single source/drain implants but leads to high simulation errors for deep submicron LDD-devices, especially for low voltage applications. To overcome this problem the DC and AC channel lengths are pure fitting parameters in BSIM3 V3.1 [5]. This work proposes a novel, physically based, analytical resistance model. It will be shown that with an improved bias dependent series resistance description digital and analog circuits can exactly be modeled down to sub-quarter micron channel lengths and down to supply voltages of $V_{dd}=1\,\mathrm{V}$.

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2. MEASUREMENTS AND PARAMETER EXTRACTION

Many publications, e.g. [8, 10], determine the parasitic resistances as a function of the effective channel length by using an interception method. Contrary to this we extracted the resistances of a $0.25\,\mu\mathrm{m}(=l_{des})$ technology using the geometric lengths [3]: From $C(V)$ measurements we obtained an overlap length of $2\,l_{ov}=85\,\mathrm{nm}$ (fig. 1 and 2) and a poly gate length of $l_{poly}=270\,\mathrm{nm}$. The latter was also verified by SEM measurements. With the so derived channel length $l_{ch}=l_{poly}-2\,l_{ov}=185\,\mathrm{nm}$ we extracted the parasitic resistances at a low drain source voltage ($V_{DS}=50\,\mathrm{mV}$) as shown in fig. 3 and 4.
The main advantage of this procedure is that we obtain consistent geometrical values for both DC and AC description. Due to the scalability of the resistance parameters a worst case analysis is possible.

3. ANALYTICAL SERIES RESISTANCE MODEL

It is well known from literature [9] that the parasitic series resistances R_S and R_D at source and drain are bias dependent, especially when lightly doped extentions are used to suppress short channel effects. Fig. 5 shows our used model scheme for the calculation of $R_{S/D}$. According to the resistance network the total source/drain resistor is

$$R_{S/D} \;=\; R_{ext}+\left(\frac{1}{R_{acc}}+\frac{1}{R_{spr}}\right)^{-1}+R_{dep}.$$

Device simulations show that the resistance from the source contact to the gate edge has such a weak bias dependence that a voltage independent resistance description R_{ext} is sufficient.

In the overlap region the gate voltage $V_{GS/GD}$ strongly modulates the carrier concentration by forming an accumulation layer at the $\mathsf{Si-SiO_2}$ interface when $V_{GS} > V_{FBov}$, where $V_{FBov} \approx \phi_t \cdot \ln\left(\bar{N}_{S/D}/N_{Gate}\right)$ is the flatband voltage of the overlap region [1]. The variable ϕ_t represents the thermal voltage, N_{Gate} and $N_{S/D}$ the gate and the averaged source (drain) doping concentration, respectively. In the depletion region the current can only flow through this accumulation layer (R_{dep}), while in the rest of the overlap region the current can be split into two components (fig. 5): a spreading part (R_{spr}) which depends on the doping profile [2] and a part (R_{acc}) caused by the gate induced accumulation of carriers. Neglecting the lateral field component in the depletion region the resistance R_{dep} is

$$R_{dep}(V_{GS/GD}, V_{BS}) \;=\; \frac{x_{dep}}{w\mu_n C'_{ox}\,(V_{GS/GD} - V_{FBov})}$$

with

$$x_{dep} = \sqrt{\frac{2\,\varepsilon_0\varepsilon_{si}}{q\bar{N}_{S/D}\left(1+\frac{\bar{N}_{S/D}}{N_A}\right)}\left(-V_{BS}+\phi_t\,\ln\frac{N_A\,\bar{N}_{S/D}}{n_i^2}\right)}.$$

The resistance from the end of the space charge region to the gate edge can be modeled as

$$\left(\frac{1}{R_{acc}(V_{GS/GD})}+\frac{1}{R_{spr}}\right)^{-1} = \frac{1}{w\mu_n q\alpha\bar{N}_{S/D}}\cdot\ln\left(1+\frac{q\alpha\bar{N}_{S/D}(l_{ov}-x_{dep})}{C'_{ox}(V_{GS/GD}-V_{FBov})}\right).$$

Hereby, the derivation consists of two steps. At first, the two differential resistance components $\mathrm{d}R_{acc}$ and $\mathrm{d}R_{spr}$ are connected in parallel and integrated over the spreading angle α. A second integration over the radius r provides the equation above.

The comparison of simulation and measurement data demonstrates the validity of the introduced series resistance model (fig. 4). In comparison, the BSIM3 V3.1 description which strongly underestimates the resistance for low gate voltages is also included. As resistance extraction methods fail at higher drain source biases and at separating R_S from R_D we performed MEDICI simulations which proved our model (fig. 6).

4. INFLUENCE ON CIRCUIT SIMULATION

To demonstrate the influence of the series resistances on the device characteristics we implemented our new model into BSIM3 V3.1 and simulated transfer and output curves using the results of fig. 4 as well as bias independent series resistances $R_S = R_D = 210\,\Omega\,\mu$m (fig. 7–9). To evaluate the influence of the bias dependent series resistances on the delay time of digital circuits a 17-stage $0.25\,\mu$m-CMOS ring oscillator was analysed. Taking into account all parasitics and interconnections, we compared the measured frequency ($f = 535\,$MHz $\Rightarrow$ delay time $\tau_d = 55\,$ps at $V_{dd} = 2.5\,$V) with the circuit simulation results. A good agreement can be achieved using the introduced voltage dependent series resistances for all supply voltages down to $V_{dd}=1\,$V, whereas with constant series resistances sufficient results can only be obtained at the maximum supply voltage $V_{dd} = 2.5\,$V. Fig. 10 shows that an error of nearly 30 % occurs using bias independent series resistances.
In the original BSIM3 V3.1 model these simulation errors can only be reduced by fitting the effective channel length in the DC and AC model. Due to the incorrect R_S and R_D calculation, however, the inversion charge and with it the capacitances can not be simulated correctly:

$$\begin{aligned} Q_{inv} &\sim w\cdot l\cdot C'_{ox}\,(V_{GS^*} - V_{th}) \\ &= w\cdot l\cdot C'_{ox}\,(V_{GS} - R_S I_{DS} - V_{th})\,. \end{aligned}$$

Therefore, sufficient simulation results over the entire supply voltage range ($V_{dd}=1\,\mathrm{V}\ldots2.5\,\mathrm{V}$) can not be achieved.

Not only for digital but also for analog circuit applications the correct modeling of R_S and R_D plays a key role. An example (fig. 11) demonstrates the influence on a typical analog operating point.

5. CONCLUSION

An analytical source and drain resistance model is proposed consisting only of physical parameters. With an increase of less than 2 % in CPU time it offers the opportunity to describe the DC, AC and transient behavior of MOSFETs consistently. Measurements show good agreement with our model down to subquarter micron and low power/low voltage applications.

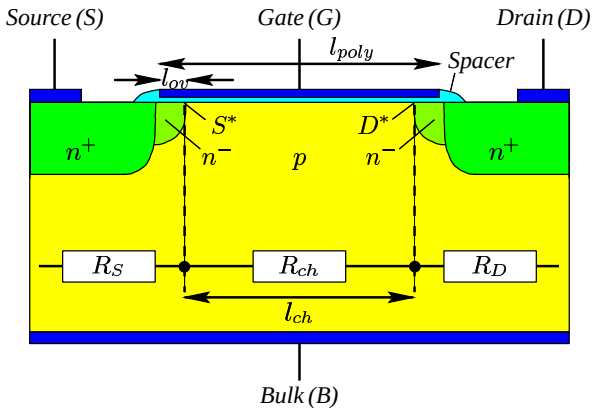

Figure 1: Source and drain resistances.

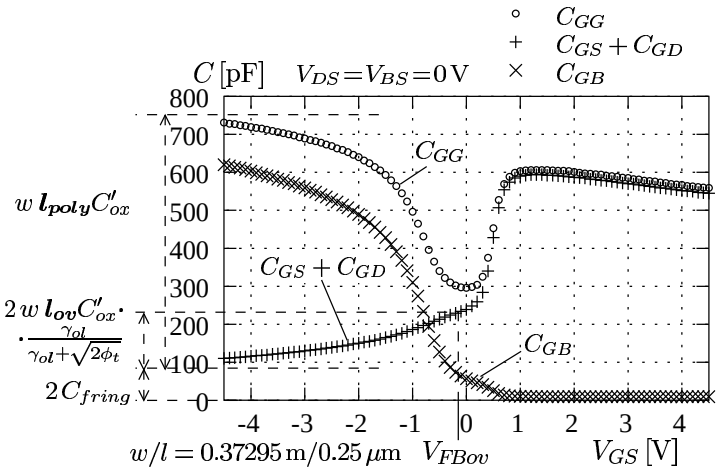

Figure 2: Extraction of the overlap length l_{ov} from measured capacitances of a quarter micron technology.

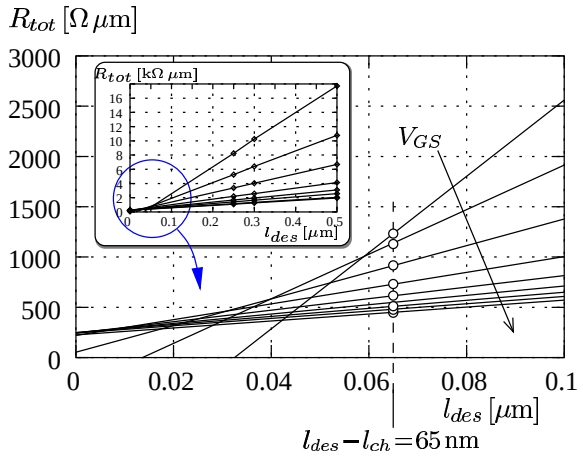

Figure 3: Extraction of the series resistances R_S+R_D.

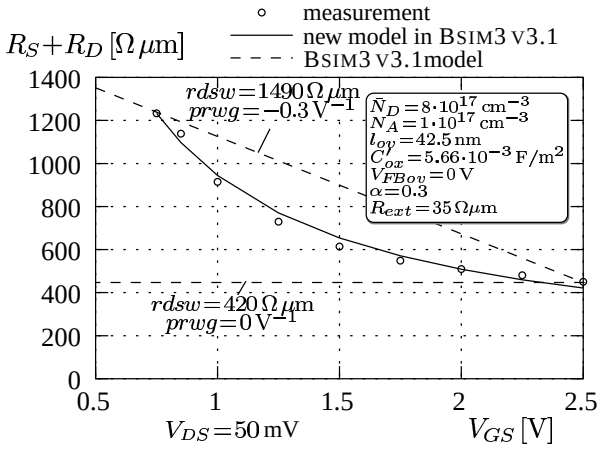

Figure 4: Series resistances R_S+R_D of a quarter micron technology, for the definition of *rdsw* and *prwg* see BSIM3 v3.1 manual [5].

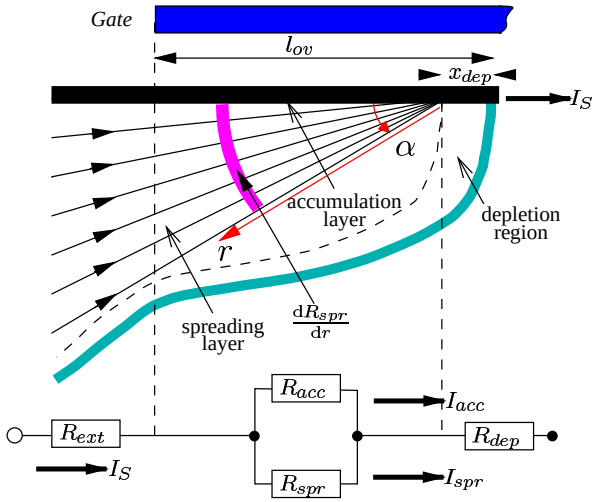

Figure 5: Model scheme and equivalent resistance network of the source side.

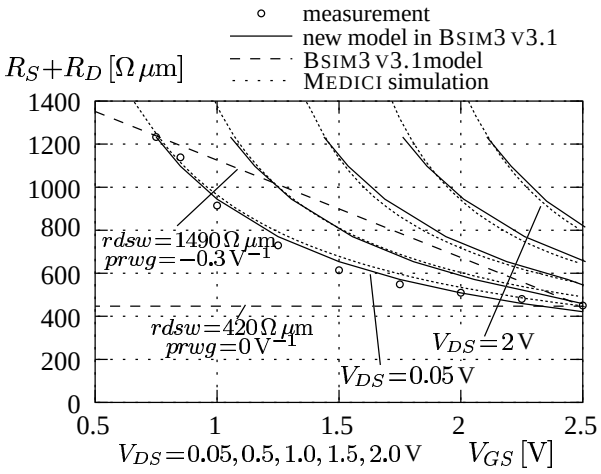

Figure 6: Comparison of MEDICI simulated source/drain resistance with new model and BSIM3 v3.1.

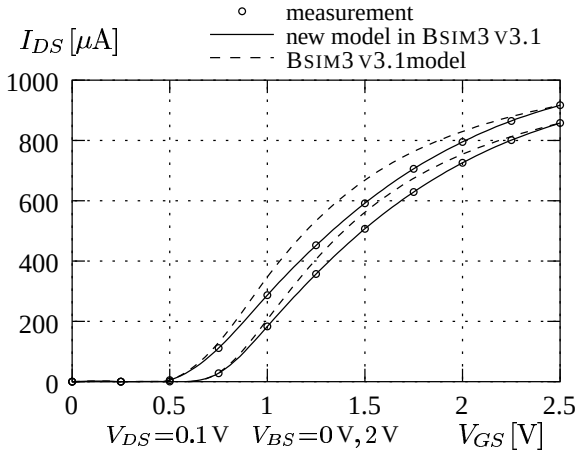

Figure 7: Transfer characteristics of a test structure with $w/l=10\,\mu\mathrm{m}/0.25\,\mu\mathrm{m}$.

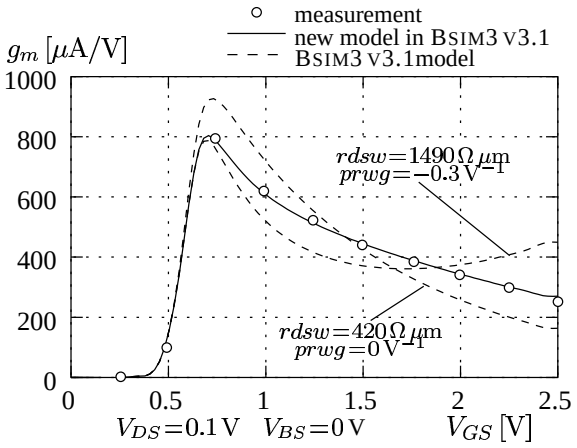

Figure 8: Transconductance of a test structure with w/l=10 μm/0.25 μm.

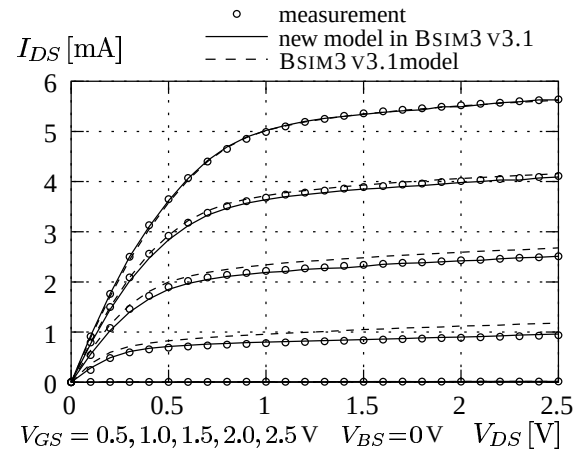

Figure 9: Output characteristic of a test structure with w/l=10 μm/0.25 μm.

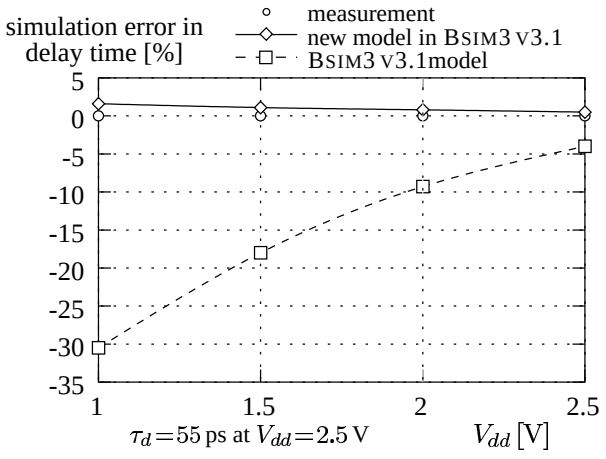

Figure 10: Comparison of measured and simulated CMOS inverter delay times at different supply voltages using different series resistances models.

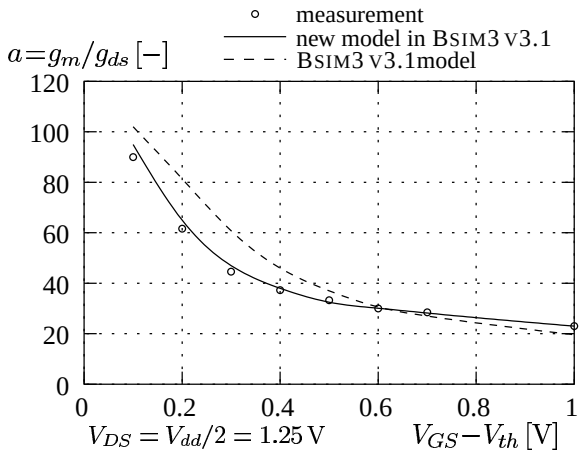

Figure 11: Comparison of measured and simulated CMOS amplification of a test structure (w/l=10 μm/0.25 μm).

6. REFERENCES

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