A Compact Model for Depletion MOSFETs in Smart Power Applications Including Source and Drain Resistance

L. Göhler, K. Kelting*

Universität der Bundeswehr München, Werner-Heisenberg-Weg 39, 85577 Neubiberg, Germany
Tel.: +49 +89 6004-3665, Fax: +49 +89 6004-2223, email: Lutz.Goehler@UniBw-Muenchen.De

*Siemens AG, HL PSE CAD, P.O. Box 801709, Balanstraße 73, D-81617 München, Germany
Tel.: +49 +89 636-22091, Fax: +49 +89 636-23147, email: Klaus.Kelting@Hl.Siemens.De

Abstract–This paper presents a compact depletion MOSFET model applicable in smart power circuit simulations. For the first time, a complete description of all internal states and the stored charge in both on-state and subthreshold region of a DMOSFET including source and drain resistance is derived. The equation set consists of explicit expressions and requires 25 parameters only.

I. Introduction

In the beginning of circuit integration depletion MOSFETs were widely used as voltage controlled resistances in NMOS inverters. Although CMOS technology dominates microelectronics today, depletion MOSFETs are still very important for circuits the power consumption of which does not play a major role. Smart power technology offers one field of use, because mainly the power semiconductors generate power losses. DMOSFETs also very often serve as current sources with $V_{GS} = V_{SB} = 0\text{V}$ in automotive ICs.

A few low voltage DMOSFET models are to be found in literature, but unfortunately they are either incomplete or suggest implicit equation systems, which consume much calculation time and tend to numerical instability. Additionally, there is no model of a high voltage DMOSFET hitherto.

As an example, [1] nearly completely models the behaviour except accumulation punch-through and subthreshold operation. Dynamic simulations rely on a capacitance network. In contrast to this, [5] presents implicit equations. Formulae for the source and drain charge are not given.

The following describes a model, which covers all operation regimes. It consists of a DC and a charge part, both for on-state and subthreshold mode. The charge model is based on the exact charge partition by [4]. In case of low voltage devices the equation system is explicit. The very low number of parameters ensures practical usefulness, since not more than 25 parameters have to be determined with the help of several computer-based optimization procedures.

II. Depletion MOSFET

Depletion MOSFETs of n-type are n-channel enhancement MOSFETs with an additional n-implantation as drawn in Fig. 1. To avoid oxide breakdown, high voltage devices show zones of increased insulator thickness near the drain and source terminal. In good approximation there is no gate influence on these resistances. Low voltage devices do not need such regions, hence the gate overlaps both the darin and source n^+-area at the same oxide thickness as in the middle of the device.

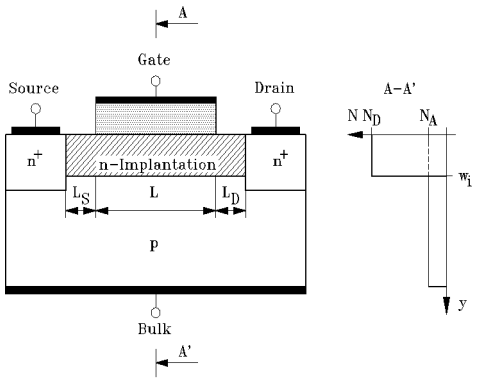

Fig. 1. Structure of a depletion MOSFET with source and drain resistance.

As known from the enhancement MOSFET there are three possible states at the semiconductor surface: accumulation, depletion and inversion. These local modes combine to six different operating conditions in the inner depletion MOSFET (Fig. 2-7). For a sweep of the gate-source voltage V_{GS} at fixed drain-source and source-bulk voltage (V_{DS}, V_{SB}) the device goes through all states in the given sequence (with exception of Fig. 4).

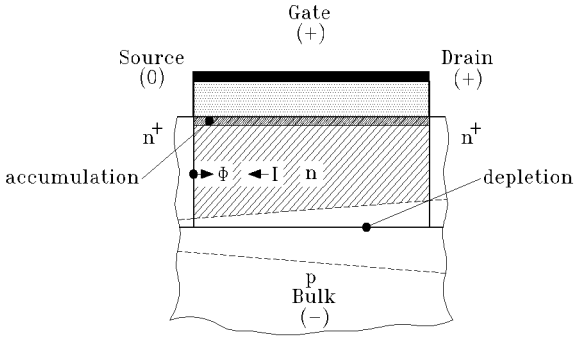

Fig. 2. Accumulation at the semiconductor surface.

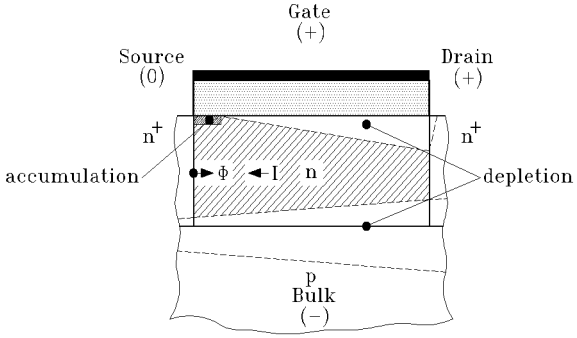

Fig. 3. Accumulation and depletion at the semiconductor surface.

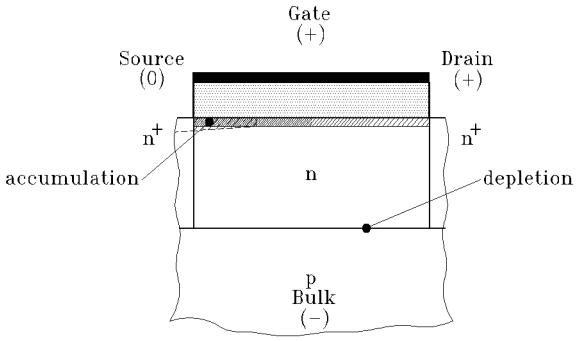

Fig. 4. Accumulation at the semiconductor surface and punch-through of body space-charge region.

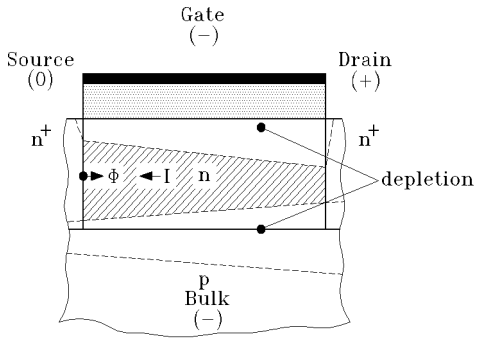

Fig. 5. Depletion at the semiconductor surface.

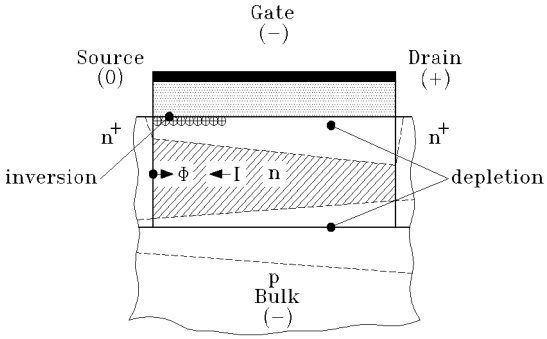

Fig. 6. Inversion and depletion at the semiconductor surface.

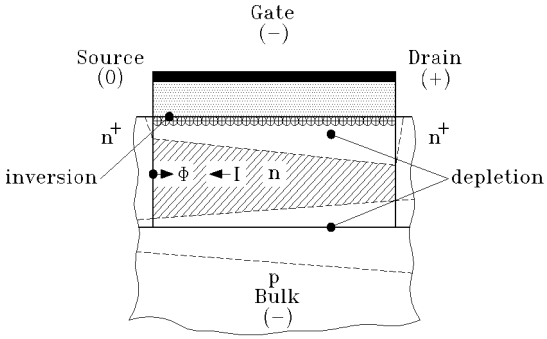

Fig. 7. Inversion at the semiconductor surface.

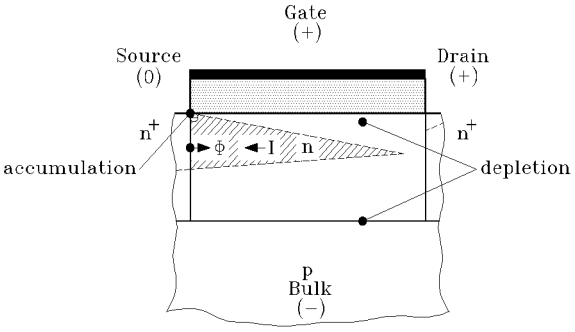

Fig. 8. Saturation for accumulation and depletion at the semiconductor surface.

If there is no accumulation at the drain (Fig. 2) saturation may occur for high drain-source voltages at the drain end of the channel. Fig. 8 illustrates this assuming a combination of accumulation and depletion under the gate oxide.

The appearance of local modes can be seen as the main difference to enhancement MOSFETs, where there is only inversion in on-state possibly turning into saturation.

Concerning the source and drain resistance depletion by the bulk space charge region predominates. The drain resistance has an additional saturation region near the terminal, when the depleted zone reaches the semiconductor surface.

Each terminal of the device can get a charge assigned. The gate charge is simply the sum over all charges on the gate metallization, whereas bulk doping ions (N_A^-) form the bulk charge. All electrons in the inner transistor and both resistances can be divided into a source and drain component (Fig. 9).

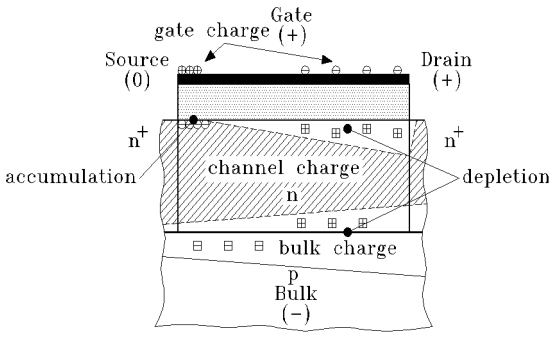

Fig. 9. Charges in a depletion MOSFET.

In subthreshold mode the electrostatic potential in the inner transistor remains approximately constant along the channel, thus the current flows mainly by diffusion of very few electrons.

Based on these considerations a model description will be derived in the next section.

III. Model Description

The key to a compact circuit model is the introduction of an electrostatic potential Φ (Fig. 2-8) and the definition of individual charges per area for each possible state at the semiconductor surface:

- accumulation ($Q_{na}^{'}$)
- accumulation punch-through ($Q_{nap}^{'}$)
- depletion (Q_{nd})
- inversion (Q_{ni}).

This leads to a single equation for the drain-source current I_{DS} in on-state due to drift

$$\begin{aligned} I_{DS} &= \frac{w\mu_{ns}}{L}\left(\int_{acc.} Q_{na}^{'}\,\mathrm{d}\Phi + \int_{acc.\,pt.} Q_{nap}^{'}\,\mathrm{d}\Phi\right) \\ &\quad + \frac{w\mu_n}{L}\left(\int_{dep.} Q_{nd}^{'}\,\mathrm{d}\Phi + \int_{inv.} Q_{ni}^{'}\,\mathrm{d}\Phi\right), \end{aligned} \quad (1)$$

where w and L is the width and length of the inner transistor, respectively. With μ_n and μ_{ns} the different mobilities in the channel and at the semiconductor surface are taken into account. Both borders of each section, i.e. the limits of each integral, can be calculated in terms of Φ. A set of switching conditions assigns the proper values at each operating point. The intention is, that only those integrals applicable to a particular terminal voltage are evaluated, whereas the other terms of (1) vanish.

Source and drain resistance are only subject to partial depletion by the bulk space charge region. Hence, their current-voltage relation is

$$\begin{aligned} I_{DS} &= \frac{w\mu_n}{L_{S,D}}\int_{R_S,R_D} Q_{nRS,D}^{'}\,\mathrm{d}\Phi \\ &= \frac{w\mu_n}{L_{S,D}}\left(qN_D w_i\left(\Phi_{eS,D}-\Phi_{bS,D}\right)\right. \\ &\quad - \frac{2}{3}\sqrt{\frac{2q\varepsilon_0\varepsilon_{Si}N_AN_D}{N_A+N_D}}\left(\left(V_{SB}^*+V_D+\Phi_{eS,D}\right)^{\frac{3}{2}}\right. \\ &\quad \left.\left.-\left(V_{SB}^*+V_D+\Phi_{bS,D}\right)^{\frac{3}{2}}\right)\right), \end{aligned} \quad (2)$$

using $\Phi_{bS,D}$ as the potential Φ at the beginning and $\Phi_{eS,D}$ as the value of Φ at the end of the particular resistance. L_S and L_D is the length of the source and drain resistance, respectively (Fig. 1). Saturation in the drain resistance occurs for:

$$\Phi = \Phi_{sat} = \frac{qw_i^2N_D\left(N_A+N_D\right)}{2\varepsilon_0\varepsilon_{Si}N_A} - V_{SB}^* - V_D - V_{DS}^*. \quad (3)$$

V_{SB}^* and V_{DS}^* denote terminal voltages of the inner transistor.

Charge calculation in on-state requires an integration over the length of each particular local mode. With the known current I_{DS} the length dependence can be transformed into a potential (Φ) dependence. For the channel and bulk charge results:

$$Q_n = -\frac{w^2\mu_n}{I_{DS}}\int_0^{V_{DS}} Q_n^{'}\,Q_n^{'*}\,\mathrm{d}\Phi, \quad (4)$$

$$Q_B = -\frac{w^2\mu_n}{I_{DS}}\int_0^{V_{DS}} Q_B^{'}\,Q_n^{'*}\,\mathrm{d}\Phi. \quad (5)$$

Note that $Q_n^{'*}$ was used instead of $Q_n^{'}$ to distinguish between μ_n and μ_{ns}. From a modification of [4] the source charge follows as (see also Fig. 1):

$$\begin{aligned} Q_S &= -\frac{w^3\mu_n^2}{I_{DS}^2\left(L_S+L+L_D\right)} \\ &\quad \times \int_0^{V_{DS}} Q_n^{'*}\int_0^{\Phi} Q_n^{'}\,Q_n^{'*}\,\mathrm{d}\Phi^*\,\mathrm{d}\Phi. \end{aligned} \quad (6)$$

When defining Q_{niT} and Q_{SiT} as the channel and source charge of the inner transistor and $Q_{nS,D}^{'}$ as the channel charge per area in the resistances (6) changes to:

$$Q_S = -\frac{w^3\mu_n^2}{I_{DS}^2\left(L_S+L+L_D\right)}$$

$$\times \left(\int_{\Phi_{bS}}^{\Phi_{eS}} Q'_{nS} \int_{\Phi_{bS}}^{\Phi} Q'^{2}_{nS}\, \mathrm{d}\Phi^* \mathrm{d}\Phi \right.$$
$$\left. + \int_{V^*_{DS}}^{V^*_{DS}+\Phi_{eD}} Q'_{nD} \int_{V^*_{DS}}^{\Phi} Q'^{2}_{nD}\, \mathrm{d}\Phi^* \mathrm{d}\Phi \right)$$
$$+ \frac{L + L_D}{L_S + L + L_D} Q_{nS} + \frac{L}{L_S + L + L_D} Q_{SiT}$$
$$+ \frac{L_D}{L_S + L + L_D} Q_{niT}. \quad (7)$$

All charges sum up to zero:

$$0 = Q_G + Q_B + Q_n - Q_i \quad (8)$$

with

$$Q_i = -qww_i L N_D\,. \quad (9)$$

Approximating all square roots by a terminated Taylor series drastically simplifies the equations for the charge model with only a slight loss of accuracy.

In subthreshold operation the channel is cut off over its whole length. The remaining electrons transport the current by diffusion. Boltzmann's statistics predict an exponential behaviour of I_{DS} for constant $\Phi = \Phi_s$ but varying electrochemical potential:

$$I_{DS} = \frac{w}{L} I_s \exp\left(\frac{\Phi_s}{V_T}\right)\left(1 - \exp\left(-\frac{V^*_{DS}}{V_T}\right)\right). \quad (10)$$

In contrast to [3] we need only one additional parameter instead of three. Since diffusion predominates grad(n) is constant, which makes the charge calculation for the inner transistor easier:

$$Q_{niT} = Q_s \exp\left(\frac{\Phi_s}{V_T}\right)\left(1 + \exp\left(-\frac{V^*_{DS}}{V_T}\right)\right), \quad (11)$$

$$Q_s = -\frac{1}{2}\frac{wL}{\mu_n V_T} I_s,$$

$$Q_{BiT} \approx Q_{Bs}\sqrt{\Phi_s + V_D + V^*_{SB}}, \quad (12)$$

$$Q_{Bs} = -wL\sqrt{\frac{2q\varepsilon_0\varepsilon_{Si} N_A N_D}{N_A + N_D}},$$

$$Q_{SiT} = \frac{Q_s}{3}\exp\left(\frac{\Phi_s}{V_T}\right)\left(2 + \exp\left(-\frac{V^*_{DS}}{V_T}\right)\right). \quad (13)$$

Beside the basic current and charge description our model includes:

- channel length modulation
- avalanche breakdown
- parasitic diodes (source/drain-bulk junction)
- temperature dependence of all currents and charges (e. g. $I_s = f(T)$, $\mu_{n,ns} = f(T)$).

The 25 paramters can be determined automatically. Reference [2] explains the strategy more detailed. Not all parameters need to be known for each device. As an example, the parasitic diodes of the source and drain region exhibit a small influence on the terminal characteristics of a long channel DMOSFET only.

IV. Results

The model was implemented in a *SABER* simulator. For verification simulated output and transfer characteristic are compared with measurements (Fig. 10, 11). Both figures proof a good model quality. Deviations are mainly due to the assumption of an abrupt junction between channel and bulk (as in [1], [5]).

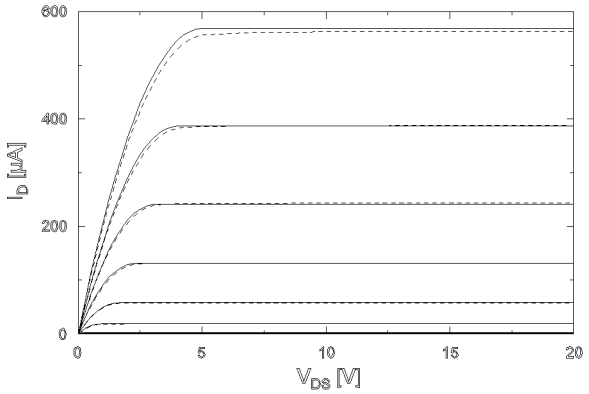

Fig. 10. Output characteristic of a DMOSFET *with* source and drain resistance (- - measured, — simulated; $V_{GS} = (-3 \ldots 5)$V, $V_{SB} = 0$V).

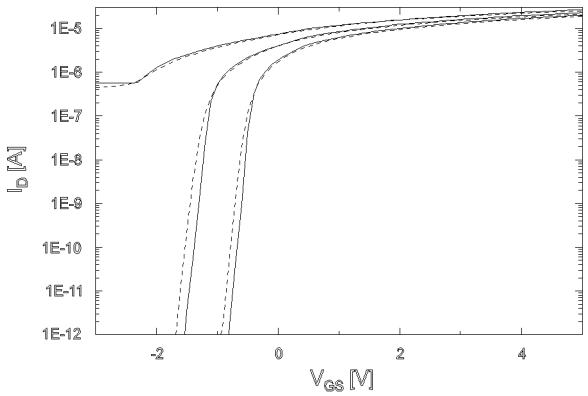

Fig. 11. Transfer characteristic of a DMOSFET *with* source and drain resistance (- - measured, — simulated; $V_{DS} = 0.1$V, $V_{SB} = (0 \ldots 5)$V).

Capacitance measurements provide a suitable benchmark for the charge model. We measured and simulated

the gate-gate capacitance G_{GG}, which is defined to be

$$C_{GG} = \left.\frac{\mathrm{d}Q_G}{\mathrm{d}V_{GS}}\right|_{V_{SB},V_{DB}=\text{const.}} \tag{14}$$

at $V_{SB} = V_{DB} = 0\text{V}$ for a device without additional resistances. Both curves show some differences caused by the already mentioned doping profile approximation and a sharp transition between various semiconductor surface states. The last simplification is absolutely necessary to obtain integrable electron charges per area in (1) and hence an explicit equation system of the inner device.

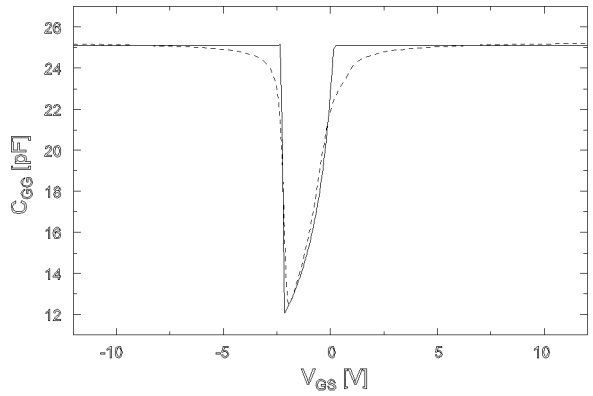

Fig. 12. Gate-gate capacitance of a DMOSFET *without* source and drain resistance (- - measured, — simulated; $V_{SB} = V_{DS} = 0\text{V}$).

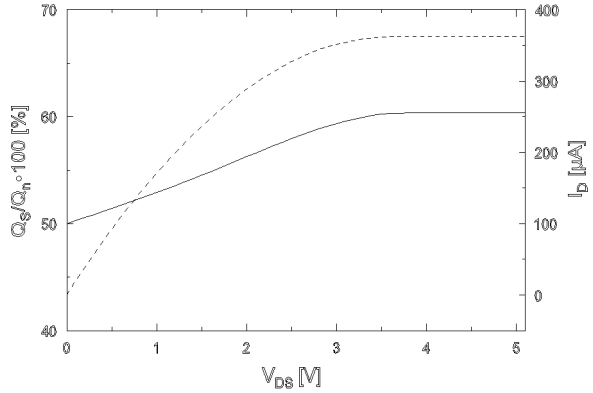

Fig. 13. Drain current (- -) and source charge in per cent of channel charge (—) of a DMOSFET *without* source and drain resistance ($V_{SB} = 0\text{V}$, $V_{GS} = 3\text{V}$).

Finally, Fig. 13 displays the drain current and the ratio between source and channel charge again for a device without source and drain resistance. It can be seen, that source and drain charge are equal at $V_{DS} = 0$, since the surface state and the bulk depletion region width do not change along the channel. With rising V_{DS} there are fewer electrons at the drain than near the source, because the space charge region width increases. Eventually pinch-off occurs and the source and drain charge ratio assumes a value of $Q_S/Q_D \approx 1.5$.

V. Conclusion

A depletion MOSFET model for smart power circuit simulations covering all operation modes was presented. It applys a charge description for all internal states in subthreshold mode and on-state.

Measurements of DC characteristics and capacitances prove the validity of the description.

All 25 parameters can be determined automatically, which guarantees practical usefulness.

References

[1] Youssef A. El-Mansy, "Analysis and Characterization of the Depletion-Mode IGFET"; IEEE Transactions on Electron Devices, pp. 331-340, 1980.

[2] Lutz Göhler, Klaus Kelting, "A Scalable Compact Model for Depletion MOSFETs in Smart Power Applications Allowing Efficient Parameter Determination"; to be published at COBEP '99.

[3] Thomas E. Hendrickson, "A Simplified Model for Subpinchoff Conduction in Depletion-Mode IGFET's"; IEEE Transactions on Electron Devices, pp. 435-441, 1978.

[4] Soo-Young Oh, Donald E. Ward, Robert W. Dutton, "Transient Analysis of MOS Transistors"; IEEE Transactions on Electron Devices, pp. 1571-1578, 1980.

[5] Claudio Turchetti, Guido Masetti, "Analysis of the Depletion-Mode MOSFET Including Diffusion and Drift Currents"; IEEE Transactions on Electron Devices, pp. 773-782, 1985.