A Unified Compact Model for Depletion MOSFETs in Smart Power Applications

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Abstract

This paper presents a compact depletion MOSFET (DMOSFET) model primary applicable in smart power circuit simulations. For the first time, a complete description of all internal states and the stored charge in both on - state and subthreshold operation of a DMOSFET is given. Despite these advantages the equation set requires 25 parameters only.

Introduction

In the beginning of circuit integration depletion MOSFETs were often used as load elements in inverters. Although CMOS technology replaced NMOS processes in many applications there is still a wide field of use for these traditional solutions. Obviously this development results from a high cost pressure on products the power consumption of which is a rather non - critical value. Even in smart power technology these conditions are given, because the logic part causes a small fraction of the total power losses only.
A few models of DMOSFETs are to be found in literature, but unfortunately the they do not cover all operation modes. Furthermore, some of them suggest implicit equation systems, which normally leads to numerical problems during simulation. In [1] for example, the subthreshold mode is not considered and the dynamic model relys on a capacitance network, whereas [5] presents an implicit system with an incomplete dynamic description
In the following, a model providing information on all modes is presented. Charges assigned to each device terminal allow the calculation of displacement currents for dynamic simulations.

Depletion MOSFET

A *n* - type depletion MOSFET consists of a *n* - type enhancement MOSFET with an additional *n* - implantation (buried channel). Fig. 1 shows the typical structure of a logic voltage level (e.g. 5V) element. The doping profile in the channel (*n*) and the bulk (*p*) is assumed to be homogeneous, thus forming an abrupt *pn* - junction.
Since the implantation establishs a conducting layer already at V_{GS} = 0V the device is normally on.

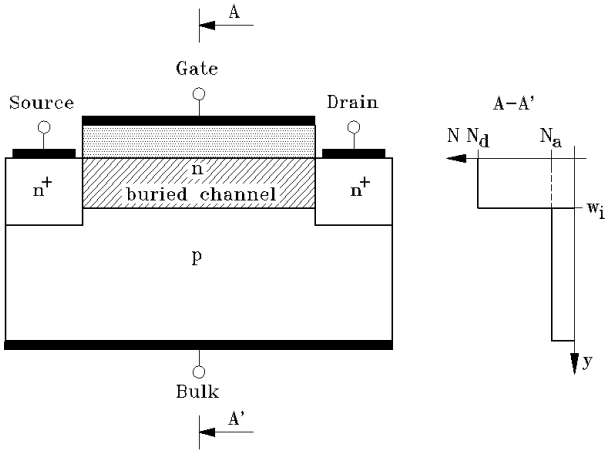

Figure 1. Structure of a *n* - type depletion MOSFET.

The three possible modes at the oxide underside (accumulation, depletion, inversion) combine to six different internal states as shown in the following figures (Fig. 2 - 8).

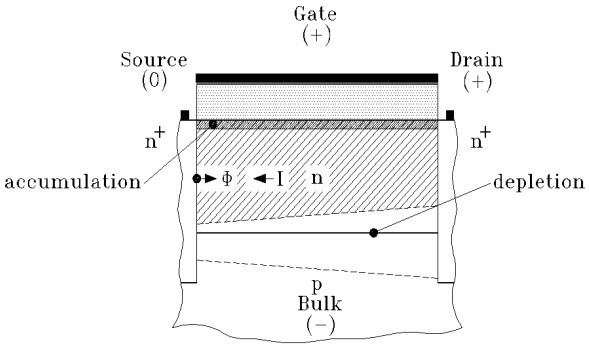

Figure 2. Accumulation at the semiconductor surface.

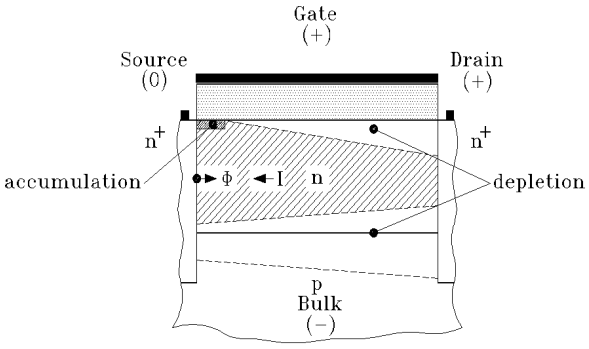

Figure 3. Accumulation and depletion at the semiconductor surface.

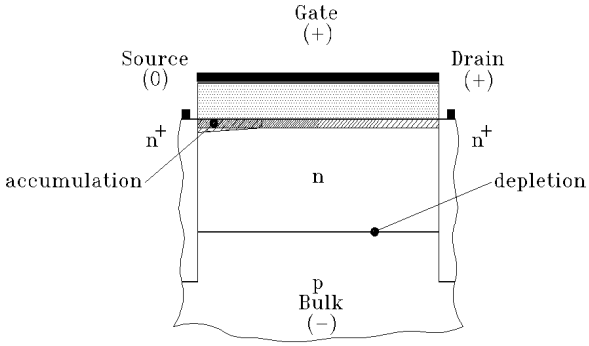

Figure 4. Accumulation at the semiconductor surface and punch - through of bulk space - charge region.

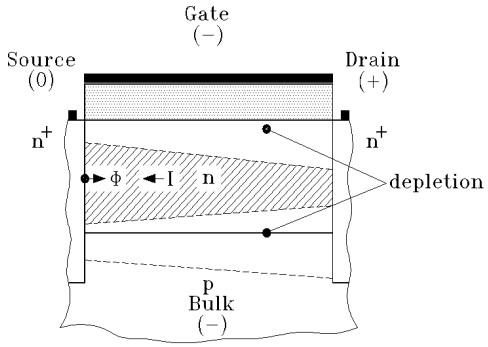

Figure 5. Depletion at the semiconductor surface.

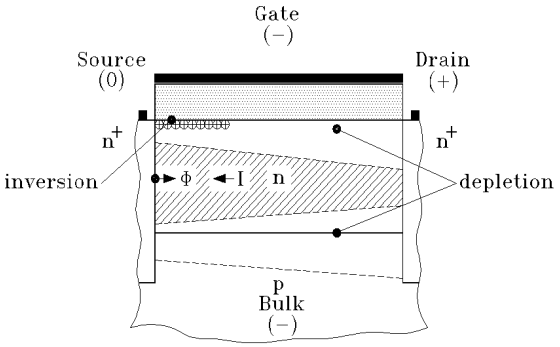

Figure 6. Depletion and inversion at the semiconductor surface.

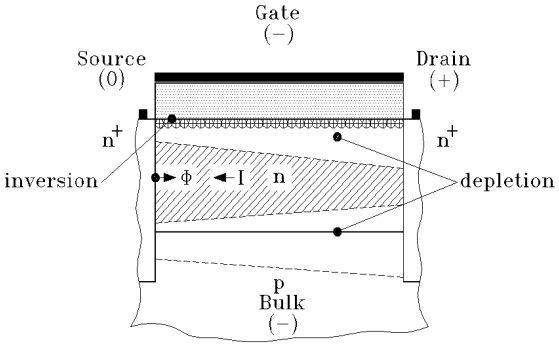

Figure 7. Inversion at the semiconductor surface.

With exception of the first case saturation may occur at the drain end of the channel. Fig. 8 illustrates this behaviour assuming a combination of accumulation and depletion (see also Fig. 3). It can be seen, that the space – charge regions from the bulk and gate cut off the channel by touching each other.

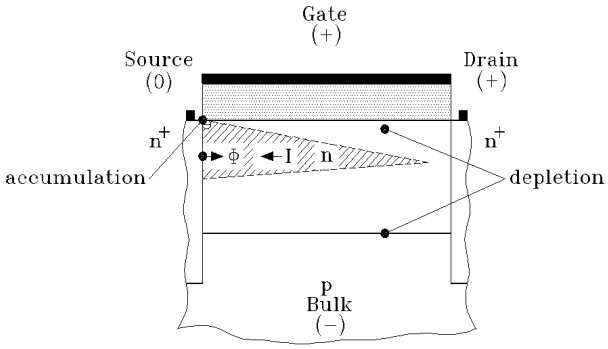

Figure 8. Saturation for accumulation and depletion at the semiconductor surface.

The several combinations of local modes are the main difference to enhancement MOSFETs, where there is only inversion in the on - state possibly turning into saturation.
With neglection of Fig. 4 all mode combinations occur in the mentioned sequence, when the gate source voltage V_{GS} changes from positive to negative values for fixed V_{DS} and V_{SB}.
In subthreshold operation the channel is cut off over its whole length. Hence, the very few remaining electrons can conduct the current by diffusion only. The onset of inversion at certain terminal conditions leads to a lower limitation of the drain - source current I_{DS}.
Each of the four terminals can get a charge assigned (Fig. 9), so that displacement currents flow during transient simulations. The gate charge is simply the sum over all charged particles on the gate metallization, whereas doping ions in the *p* - region form the bulk charge. Source and drain charge in total equal the channel charge including accumulated electrons.

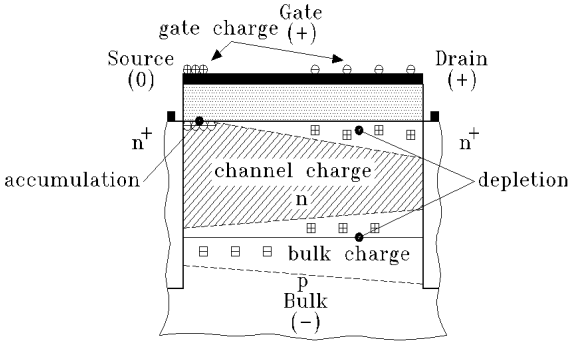

Figure 9. Charges in a depletion MOSFET.

Based on these considerations a set of model equations will be derived in the next section.

Model Description

The key to a simple model formulation is the definition of an electrostatic potential *F* in the channel as already drawn above (Fig. 2 - 8). In on - state current flows due to carrier drift, and the separation into four possible sections (accumulation (Q'_{na}), accumulation punch - through (Q'_{nap}), depletion (Q'_{nd}), inversion (Q'_{i})) with charges per area assigned accordingly yields

$$I_{DS} = \frac{w m_{ns}}{L}\left(\int_{acc.} Q'_{na}\, d\ddot{O} + \int_{acc.\,pt.} Q'_{nap}\, d\ddot{O} \right) + \frac{w m_{n}}{L}\left(\int_{dep.} Q'_{nd}\, d\ddot{O} + \int_{inv.} Q'_{ni}\, d\ddot{O} \right), \qquad (1)$$

where w and L is the width and length of the channel, respectively. The variables μ_{ns} and μ_n denote the electron mobility at the surface and in the channel. Both borders of each section, i.e. both limits of each integral, can be calculated in relation to F. A set of switching conditions assigns the proper values. The intention is, that only the integrals applicable to a particular terminal voltage condition have to be solved. As a result, all other terms of (1) vanish.
An approach like this drastically reduces the number of equations, because only four integrals have to be solved for six different states. This also affects the charge model, the equations of which are otherwise very long.
All charge calculations require information on the spatial extension of the particular local mode. Using the known current I_{DS} the length dependence can be transformed into a potential dependence in terms of F.
Channel (Q_n) and bulk charge (Q_B) for drift result in:

$$Q_n = -\frac{w^2 \mu_n}{I_{DS}} \int_0^{V_{DS}} Q'_n \, Q'^*_n \, d\ddot{O}, \tag{2}$$

$$Q_B = -\frac{w^2 \mu_n}{I_{DS}} \int_0^{V_{DS}} Q'_B Q'^*_n \, d\ddot{O}. \tag{3}$$

Note that Q'^*_n was written instead Q'_n to distinguish between the two mobilities. Again, integration has to be performed over all four sections. The source charge derives from a modified approach of [4] and requires more calculation effort:

$$Q_S = -\frac{w^3 \mu_n^2}{I_{DS}^2 L} \int_0^{V_{DS}} Q'^*_n \int_0^{\Phi} Q'_n Q'^*_n \, d\ddot{O}^* \, d\ddot{O} \, . \tag{4}$$

In total, all charges sum up to zero

$$0 = Q_G + Q_B + Q_n - Q_i \, , \tag{5}$$

with

$$Q_i = -q w w_i L N_d \, . \tag{6}$$

N_d names the channel doping with a depth of w_i.(see Fig. 1) The constant q represents the elementary charge.
Inversion excepted (6) provides the gate charge. Consequently, a term considering the hole contribution has to be added in the model.
In subthreshold mode the current assumes an exponential form:

$$I_{DS} = \frac{w}{L} I_s \exp\left(\frac{\ddot{O}_s}{V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right). \tag{7}$$

I_s is a current parameter, V_T the thermal voltage and F_s the Potential F in the channel under subthreshold conditions. Its lower limit is given by the onset of inversion. Equation (7) needs 2 parameters less than the solution in [3]. The exponential form follows from Boltzmann´s statistics with the assumption of a constant electrostatical but a varying electrochemical potential between source and drain. Since diffusion predominates grad(n) does not change. This knowledge simplifies charge calculation significantly. For Q_n, Q_B and Q_S one gets:

$$Q_n = -\frac{1}{2}\frac{wL}{\mu_n V_T} I_s \exp\left(\frac{\ddot{O}_s}{V_T}\right)\left(1+\exp\left(-\frac{V_{DS}}{V_T}\right)\right), \tag{8}$$

$$Q_B \approx -wL\sqrt{\frac{2q\varepsilon_0\varepsilon_{Si}N_a N_d}{N_a+N_d}\left(\ddot{O}_s+V_D+V_{SB}\right)} \tag{9}$$

and

$$Q_S = -\frac{1}{6}\frac{wL}{\mu_n V_T} I_s \exp\left(\frac{\ddot{O}_s}{V_T}\right)\left(2+\exp\left(-\frac{V_{DS}}{V_T}\right)\right). \tag{10}$$

N_a denotes the bulk doping and V_D is called diffusion voltage (of the channel - bulk junction).
In addition to this static and dynamic description our model includes:

- channel length modulation
- breakdown
- parasitic diodes formed by the source/drain - bulk junction (n^+ - p)
- temperature dependence of all currents and charges (e.g. $I_s = f(T)$, μ_n, $\mu_{ns} = f(T)$).

The parameter set consists of 25 values, the determination of which will be explained in [2]. Not all of them need to be known for each device. As an example, the parasitic diodes are negligible in a long channel DMOSFET.

Results

We tested the model for a long channel element with w/L = 1. Fig. 10 shows the output characteristic. Good agreement between measured and simulated behaviour could be achieved. This is also proved by the transfer characteristic (Fig. 11) plotted in a semilogarithmic scale. Deviations are mainly due to the assumption of a homogeneous doping profile, which influences the reproduction of the body effect (i.e. $I_{DS} = f(V_{SB})$).

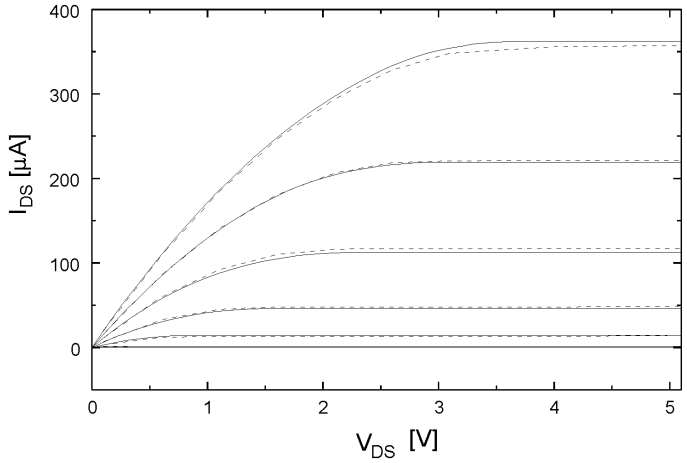

Figure 10. Output characteristic (- - measured, — simulated; V_{GS} = (-3...3)V, V_{SB} = 0V).

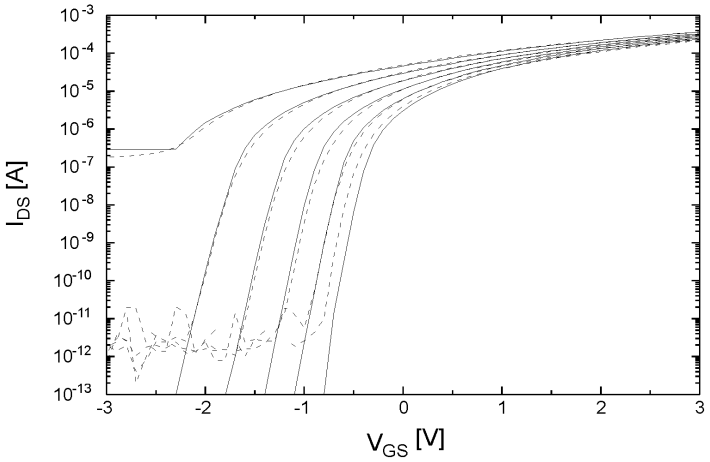

Figure 11. Transfer characteristic (- - measured, — simulated; V_{DS} = 5.1V, V_{SB} = (0...5)V).

Capacitance comparison provides a test for the charge model. We determined the gate - gate capacitance

$$C_{GG} = \left.\frac{\mathrm{d}Q_G}{\mathrm{d}V_{GS}}\right|_{V_{SB},V_{DB}=\text{const.}} \tag{11}$$

by simulation and experiment for V_{SB} = V_{DB} = 0V (Fig. 12). The differences between both curves are caused on one hand by the already mentioned doping profile approximation and on the other hand by a sharp transition between the semiconductor surface states. This last simplification is absolutely necessary to obtain integrable expressions for the individual charges in (1) and hence an explicit equation system.

Finally, Fig. 13 displays the normalized source charge for a single output curve ($Q_S/Q_n \cdot 100\% = f(V_{DS})$ at constant V_{GS}). The corresponding output curve is also to be seen. For V_{DS} = 0 source and drain charge are equal, since there is no change of the bulk space charge region width and the semiconductor surface state along the channel. With increasing drain - source voltage the drain end of the channel gets into depletion and finally in saturation. Therefore there are fewer electrons near the drain than at the source. This results in an increase of the source and drain charge ratio. In saturation this value reaches approximately $Q_S / Q_D \approx$ 1.5.

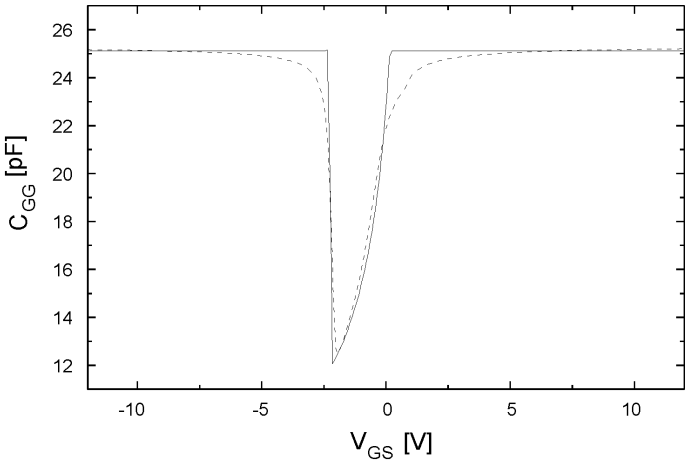

Figure 12. Gate - gate capacitance (- - measured, — simulated; V_{DS} = V_{SB} = 0V).

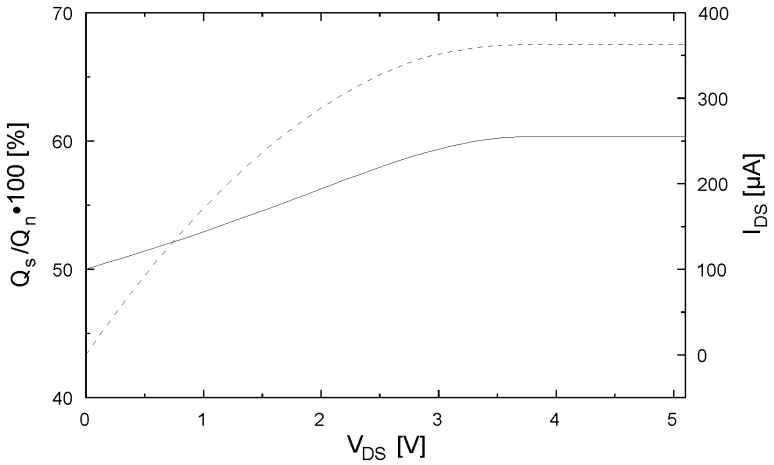

Figure 13. Drain current (- -) and source charge in per cent of channel charge (—) (V_{SB} = 0V, V_{GS} = 3V).

Conclusion

In this paper a depletion MOSFET model for smart power circuit simulations was presented. The model excels by a complete description of all internal states including subthreshold operation and a charge model for transient simulations.
Measurements prove the validity of the model. All 25 parameters can be determined automatically, so that practical usefulness is guaranteed.

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