Input and Reverse Transfer Capacitance Measurement of MOS-Gated Power Transistors under High Current Flow

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Abstract

The measurement principle of the input and reverse transfer capacitance is shown. Function, stability and operation of the measurement circuits is discussed. The on state capacitances of a power DMOS transistor were measured under high current conditions of up to 250A. A strong nonlinear characteristic is observed.

Introduction

Capacitances are normally specified in data sheets without current flow. In the on state, there are only two capacitances significant for a MOS-gated device with three pins: input and reverse transfer capacitance. The measurement principles of these characteristics will be demonstrated using a power DMOS, but can be generally used for MOS-gated transistors.

The characteristic of the reverse transfer capacitance has, due to the *Miller*-effect the most significant influence on the transient behaviour of power transistors and will be considered first.

For the measurement of C_{GD} (gate drain capacitance or respectively reverse transfer capacitance), V_{GS} (gate source voltage) is held constant and V_{DS} (drain source voltage) of the DUT (device under test) is varied. Normally this is done by applying the constant V_{DS} bias with an additive small signal sine wave. V_{GS} is held constant and I_G (gate current) is measured.

$$C_{GD} = I_G \frac{\mathrm{d}t}{\mathrm{d}V_{DS}}\bigg|_{V_{GS}=const} \tag{1}$$

This method is very accurate, but has a long T (measurement time). Applying the V_{DS} bias while there is a I_D (drain current) flowing results in the situation that $P = V_{DS}I_D$ (heating power) can not be conducted to the heat sink as quickly as required. In this case the $E = V_{DS}I_DT$ (accumulated energy) would lead to self heating and destruction of the DUT due to thermal overload.

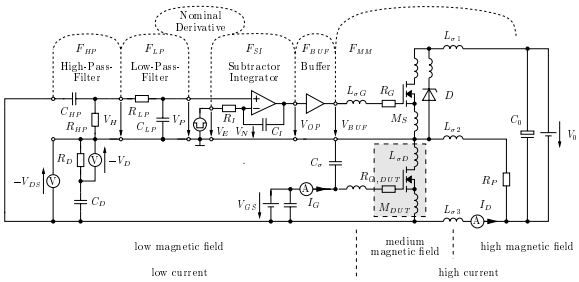

Figure 1: Basic structure of the C_{GD} measurement circuit.

The goal of the circuit (fig. 1) is to produce a short voltage ramp on the drain of the DUT replacing a sine wave. The short ramp reduces the accumulated energy tremendously and subsequent ramps are spaced with a cooling time of several seconds.

C_{GD} derives the V_{DS} ramp using the relationship $I_G = C_{GD}\frac{\mathrm{d}V_{DS}}{\mathrm{d}t}$. Because the measurement result C_{GD} is directely proportional to I_B (equ. 1), the derivative of V_{DS} must be constant.[1]

Circuit Function

Subsequent V_{DS} ramps have different V_{GS} values and are spaced by a cooling time. V_{GS} is held constant for one V_{DS} ramp. This produces a group of C_{GD} curves with continuous V_{DS} while V_{GS} is a variable.

$I_G(t)$ is measured potential free using a current probe.

All transients should be measured with one oscilloscope, so that they have the same time base and voltages of different channels are sampled at the same time. Of course

[1] If the corresponding $\frac{\mathrm{d}V_{DS}}{\mathrm{d}t}$ is measured too and used for the calculation of C_{GD} then mathematically everything is correct. Due to parasitic elements ideal measurements are not possible and experience shows that a non constant $\frac{\mathrm{d}V_{DS}}{\mathrm{d}t}$ leads to unsatisfactory results.

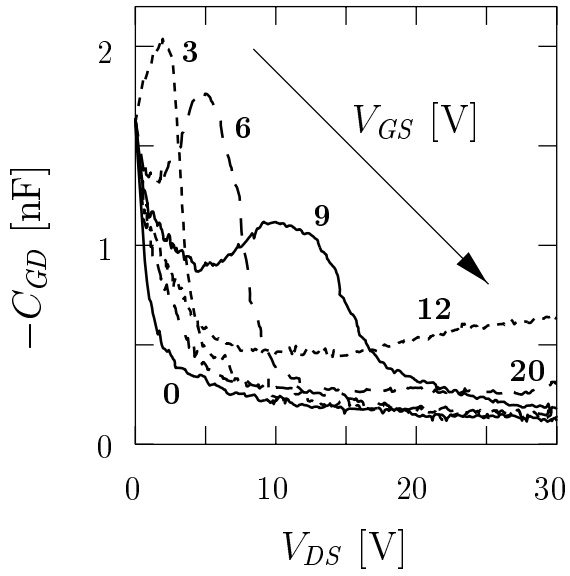

Figure 2: Measured gate-drain capacitance of the BUZ 103 SL.

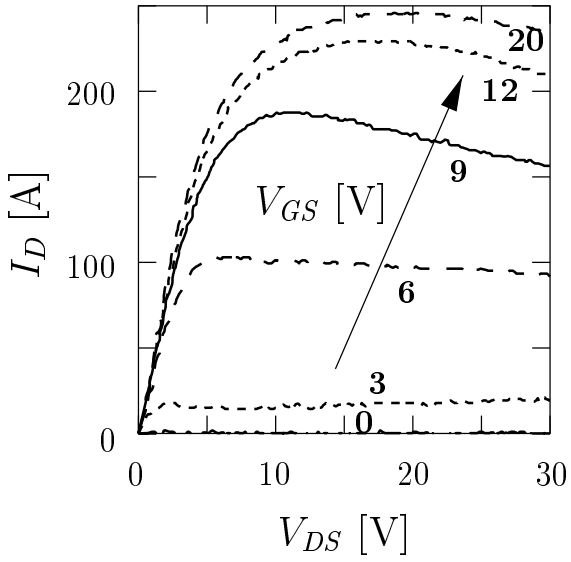

Figure 3: Measured transfer characteristic of the BUZ 103 SL.

the measured values of different channels must be the result of the same ramp event.

Because the ramp event must be triggered by a pulse generator, which has usually a common ground together with the oscilloscope via earth, this ground level is placed at the drain of M_{DUT}. During the idle time, V_E must be positive, driving V_{OP} to the negative supply voltage of the operational amplifier.

During the ramp time, $-V_{DS}(t)$ is measured.

$\frac{\mathrm{d}V_{DS}}{\mathrm{d}t}$ is measured indirecty using a known capacitance C_D between drain and source and measuring the current $\frac{V_D(t)}{R_D}$ through it using a small series resistance R_D.

$$V_D \approx \tau_D \frac{\mathrm{d}V_{DS}}{\mathrm{d}t} \tag{2}$$

$$\tau_D = R_D C_D \tag{3}$$

C_{GD} is calculated using equ. 1 and 2 (fig. 2).

$$C_{GD}(V_{GS}, V_{DS}(t)) \approx \tau_D \frac{I_G(t)}{V_D(t)}\bigg|_{V_{GS}=const} \tag{4}$$

Next the V_{DS} ramp should be supplied. This supply must be able to supply a high current. Therefore a MOS transistor M_S is connected in series to M_{DUT}. This series MOS transistor is connected to a capacitance C_0 capable of supplying the high current I_D with a high current slew rate $\frac{\mathrm{d}I_D}{\mathrm{d}t}$ and the charge $\int_0^T I_D \mathrm{d}t$ where T is the ramp time. The parasitics must be sufficiently small while the capacitance value must be large enough.

For the transfer characteristic, I_D can be measured potential free using a current probe between the source of M_{DUT} and C_0 (fig. 3). As is obvious by the slight decrease of current, self-heating was not completely avoided.

In order to supply the correct control gate voltage to the series MOS transistor corresponding to the V_{DS} ramp, a regulation circuit was constructed.

Regulation Circuit

V_{DS} is reversed and fed into a high pass filter HP (fig. 4).

$$V_H = \underbrace{\frac{p\tau_{HP}}{1+p\tau_{HP}}}_{F_{HP}}(-V_{DS}) \tag{5}$$

$$p = j2\pi f \tag{6}$$

$$\tau_{HP} = R_{HP} C_{HP} \tag{7}$$

For a frequency below

$$f_{HP} = \frac{1}{2\pi\tau_{HP}} \tag{8}$$

the output voltage of the HP is the derivative of V_{DS}.

$$V_H(f < f_{HP}) \approx p\tau_{HP}(-V_{DS}) \tag{9}$$

The output voltage of the operational amplifier can be described by

$$V_{OP} = \frac{V_P - \frac{1}{1+p\tau_I}V_E}{\frac{1}{k} + \frac{p\tau_I}{1+p\tau_I}} \tag{10}$$

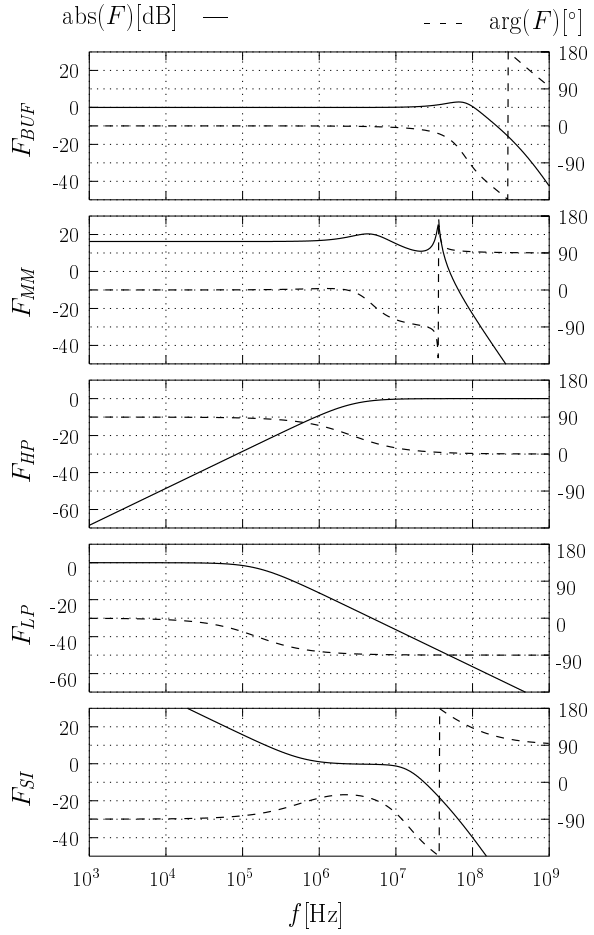

Figure 4: Open Loop Frequency Response of the Circuit Components.

$$k = \frac{V_{OP}}{V_P - V_N} \tag{11}$$

$$\tau_I = R_I C_I \tag{12}$$

The regulation principle is demonstrated now by removing the low-pass-filter and connecting the output of the high-pass-filter directely to the subtractor-integrator part ($V_P = V_H$, equn. 13 to 15).

$$V_{OP} = \frac{\frac{p\tau_{HP}}{1+p\tau_{HP}}(-V_{DS}) - \frac{1}{1+p\tau_1}V_E}{\frac{1}{k} + \frac{p\tau_1}{1+p\tau_1}} \tag{13}$$

Using an ideal operational amplifier this results in

$$\lim_{k\to\infty} V_{OP} = \frac{\tau_{HP}(1+p\tau_I)}{\tau_I(1+p\tau_{HP})}(-V_{DS}) - \frac{1}{p\tau_I}V_E \tag{14}$$

Additionally, when choosing the same time constant for τ_{HP} and τ_I

$$-V_E = p\tau\left(V_{DS} + \lim_{k\to\infty} V_{OP}\Big|_{\tau_{HP}=\tau_I=\tau}\right) \tag{15}$$

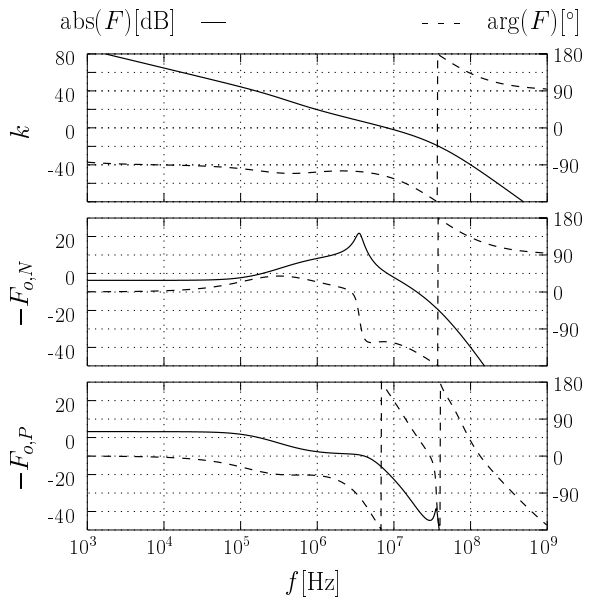

Figure 5: Open Loop Frequency Response of the Operational Amplifier and Regulation Circuit.

it can be shown, that the difference between the real derivative $\frac{\mathrm{d}V_{DS}}{\mathrm{d}t}$ and the nominal derivative, which is adjusted by V_E, is integrated and fed into the gate of M_S.

So, when $\frac{\mathrm{d}V_{DS}}{\mathrm{d}t}$ becomes smaller, the gate voltage of M_S is rising faster, resulting in a faster pull up of V_{DS}.

In order to keep the deviation from the nominal derivative small, the gain $F_{MM} = \frac{V_{DS}}{V_{BUF}}$ must be as large as possible.

$$F_{MM} = \frac{g_{m,M_S}(R_{DS} + pL_{\sigma D})(R_P + pL_{\sigma 2})}{(1 + p\tau_R + p^2\tau_L^2)(R_{DS} + R_P + pL_\sigma)} \tag{16}$$

$$\tau_R = R_G C_G \tag{17}$$

$$\tau_L^2 = L_{\sigma G} C_G \tag{18}$$

$$L_\sigma = L_{\sigma D} + L_{\sigma 2} + L_{\sigma 3} \tag{19}$$

where R_{DS} is the small signal resistance of M_{DUT} and g_{m,M_S} is the gate transconductance, R_G is the parasitic gate resistance and C_G is the gate capacitance of M_S.[2] The parallel resisor R_P is needed for limiting the open loop gain in case of M_{DUT} saturation. $L_{\sigma 1}$ has no effect, because M_S is always in saturation.[3]

For the regulation circuit stability, both loops, ending at the positive and the negative input of the operational amplifier, must be considered (fig. 5).

$$-F_{o,N} = \frac{p\tau_I}{(1+p\tau_I)(\frac{1}{k} - \frac{V_P}{V_{OP}})} \tag{20}$$

[2]The *Miller*-effect is neglected for M_S. Parasitic source inductances are neglected generally.

[3]Channel length modulation and gate-drain capacitance of M_S are neglected.

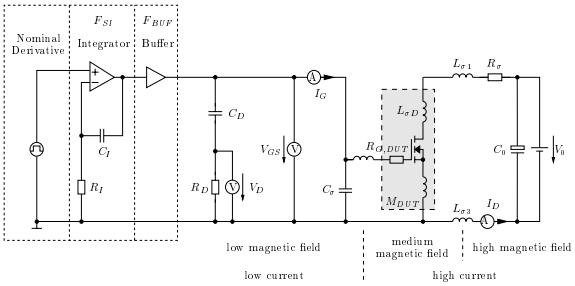

Figure 6: Basic structure of the C_{GG} measurement circuit.

$$-F_{o,P} = -\underbrace{\frac{k(1+p\tau_I)}{1+(1+k)p\tau_I}}_{F_{SI}}\frac{V_P}{V_{OP}} \quad (21)$$

$$\frac{V_P}{V_{OP}} = F_{BUF}F_{MM}(-1)F_{HP}F_{LP} \quad (22)$$

The stability is mainly affected by the parasitic inductances $L_{\sigma D}$, $L_{\sigma 2}$ and $L_{\sigma 3}$.

A low-pass-filter is inserted to increase the phase-margin.

$$F_{LP} = \frac{1}{1+p\tau_{LP}} \quad (23)$$

$$\tau_{LP} = R_{LP}C_{LP} \quad (24)$$

If M_S is switched off too fast at the end of a pulse, then its drain-source voltage may increase above the maximum blocking voltage due to the parasitic inductances. This can be avoided either by limiting the turn off speed or by adding D (transient absorbing Z-diode).

Input Capacitance

Fig. 6 shows the measurement circuit for the input capacitance, which is refered to as gate-gate capacitance in this case.

$$C_{GG} = I_G\frac{\mathrm{d}t}{\mathrm{d}V_{GS}}\bigg|_{V_{DS}=const} \quad (25)$$

Using

$$C_{GG}(V_{GS}(t),V_{DS}) \approx \tau_D\frac{I_G(t)}{V_D(t)}\bigg|_{V_{DS}=const} \quad (26)$$

the result of this measurement is shown in fig. 7.

The stability of this circuit is easily achived without long calculations.

The $L_{\sigma 1}$, $L_{\sigma 3}$ and $L_{\sigma D}$ (parasitic inductances) and the R_σ (parasitic resistance) must be as small as possible, because they induce a V_{DS} drop when I_D starts flowing.

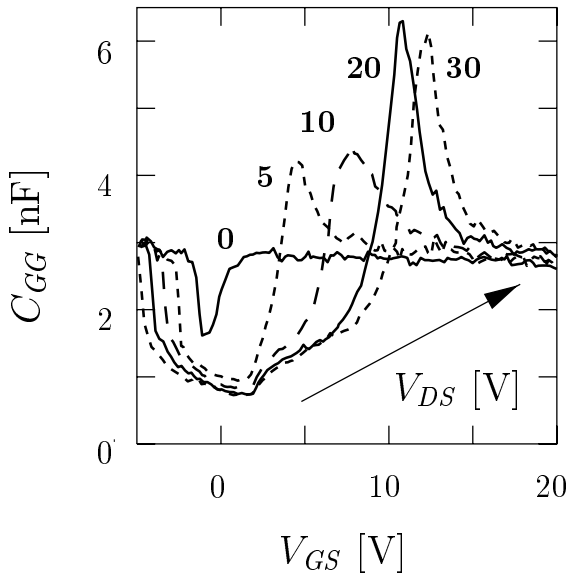

Figure 7: Measured gate-gate capacitance of the BUZ 103 SL.

Parasitics, EMC and Measurement Setup

Due to the $R_{G,DUT}$ (effective gate resistance) of the device, there is an effective voltage drop across the gate area caused by I_G.

$$V_G = R_{G,DUT}I_G \approx R_{G,DUT}C\frac{\mathrm{d}V}{\mathrm{d}t} \quad (27)$$

where C is the measured capacitance of the DUT and $\frac{\mathrm{d}V}{\mathrm{d}t}$ is the derivative of the voltage ramp. In order to keep this voltage drop between supplyed gate voltage and effective, inner gate voltage small, $\frac{\mathrm{d}V}{\mathrm{d}t}$ must be limited. For the measurements above, a slew rate of $2\frac{\mathrm{V}}{\mu\mathrm{s}}$ was chosen, leading to a worst case voltage drop of 0.17V for $R_{G,DUT} = 13\Omega$.

The resistance of the gate current probe has two effects. First this resistance must be considered by adding it to the gate resistance above. Second it causes a drop in the gate current measurement.

The wire of the DUT gate has an C_σ (parasitic capacitance) to the ground through the ribbon cable and the case of the gate current probe.

Low pass filters must be inserted between the measurement circuit and the dc voltage sources, because sources typically have parasitic capacitances to ground.

Malfunction usually ends up with destruction of all power semiconductors. Some resistances should be added to the circuits at appriproate nodes in order to achive a fail save behaviour in case of unintentional removal of the pulse generator or an incorrect sequence of connecting and disconnecting the power supplies.

A high $\frac{\mathrm{d}I}{\mathrm{d}t}$ causes an emission of a magnetic field through the parasitic inductances. In order to keep this influence

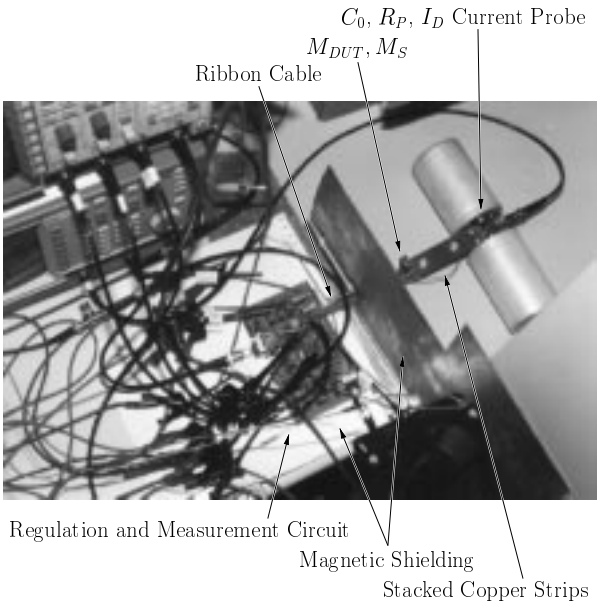

Figure 8: Measurement Setup.

on the measurement result small, the DUT is seperated from the C_0, R_P and I_D current probe using stacked copper strips insulated with a foil. The regulation and measurement circuit was additionally seperated using a ribbon cable. Both, the regulation and measurement circuit and the ribbon cable, are placed in one plane with the main magnetic field lines. The regulation and measurement circuit is shielded by two iron plates. This measurement setup is shown in fig. 8.

Reference

[1] Christoph Deml, Kurt Hoffmann: Gate-Drain Capacitance Behaviour of the DMOS Power Transistor Under High Current Flow. IEEE Power Electronics Specialists Conference. IEEE: Fukuoka 1998. Pages 1716 - 1719.