Input and Reverse Transfer Capacitance Measurement of MOS-Gated Power Transistors under High Current Flow

Christoph Deml

Infineon Technologies AG, St.-Martin-Str. 76, 81541 Munich, Germany

Abstract

The measurement principle of the input and reverse transfer capacitance is shown. Function, stability and operation of the measurement circuits is discussed. The on state capacitances of a power DMOS transistor were measured under high current conditions of up to 250A. A strong nonlinear characteristic is observed.

Introduction

Capacitances are normally specified in data sheets without current flow. In the on state, there are only two capacitances significant for a MOS-gated device with three pins: input and reverse transfer capacitance. The measurement principles of these characteristics will be demonstrated using a power DMOS, but can be generally used for MOS-gated transistors.

The characteristic of the reverse transfer capacitance has, due to the Miller-effect, the most significant influence on the transient behaviour of power transistors and will be considered first.

For the measurement of $C_{GD}$ (gate drain capacitance or respectively reverse transfer capacitance), $V_{GS}$ (gate source voltage) is held constant and $V_{DS}$ (drain source voltage) of the DUT (device under test) is varied. Normally this is done by applying the constant $V_{DS}$ bias with an additive small signal sine wave. $V_{GS}$ is held constant and $I_G$ (gate current) is measured.

$$C_{GD} = I_G \frac{dt}{dV_{DS}} \bigg|_{V_{GS}=\text{const}}$$

(1)

This method is very accurate, but has a long $T$ (measurement time). Applying the $V_{DS}$ bias while there is a $I_D$ (drain current) flowing results in the situation that $P = V_{DS}I_D$ (heating power) can not be conducted to the heat sink as quickly as required. In this case the $E = V_{DS}I_DT$ (accumulated energy) would lead to self heating and destruction of the DUT due to thermal overload.

The goal of the circuit (fig. 1) is to produce a short voltage ramp on the drain of the DUT replacing a sine wave. The short ramp reduces the accumulated energy tremendously and subsequent ramps are spaced with a cooling time of several seconds.

$C_{GD}$ derives the $V_{DS}$ ramp using the relationship $I_G = C_{GD} \frac{dV_{DS}}{dt}$. Because the measurement result $C_{GD}$ is directly proportional to $I_B$ (equ. 1), the derivative of $V_{DS}$ must be constant.\(^1\)

Circuit Function

Subsequent $V_{DS}$ ramps have different $V_{GS}$ values and are spaced by a cooling time. $V_{GS}$ is held constant for one $V_{DS}$ ramp. This produces a group of $C_{GD}$ curves with continuous $V_{DS}$ while $V_{GS}$ is a variable.

$I_G(t)$ is measured potential free using a current probe. All transients should be measured with one oscilloscope, so that they have the same time base and voltages of different channels are sampled at the same time. Of course

\(^1\)If the corresponding $\frac{dV_{DS}}{dt}$ is measured too and used for the calculation of $C_{GD}$ then mathematically everything is correct. Due to parasitic elements ideal measurements are not possible and experience shows that a non constant $\frac{dV_{DS}}{dt}$ leads to unsatisfactory results.
the measured values of different channels must be the result of the same ramp event.

Because the ramp event must be triggered by a pulse generator, which has usually a common ground together with the oscilloscope via earth, this ground level is placed at the drain of \( M_{DUT} \). During the idle time, \( V_E \) must be positive, driving \( V_{OP} \) to the negative supply voltage of the operational amplifier.

During the ramp time, \( V_{DS}(t) \) is measured.

\[
\frac{dV_{DS}}{dt} \text{ is measured indirectly using a known capacitance } C_D \text{ between drain and source and measuring the current } \frac{V_{D}(t)}{R_D} \text{ through it using a small series resistance } R_D.
\]

\[
V_D \approx \tau_D \frac{dV_{DS}}{dt} \tag{2}
\]

\[
\tau_D = R_D C_D \tag{3}
\]

\( C_{GD} \) is calculated using equ. 1 and 2 (fig. 2).

\[
C_{GD}(V_{GS}, V_{DS}(t)) \approx \tau_D \left. \frac{I_G(t)}{V_D(t)} \right|_{V_{GS}=\text{const}} \tag{4}
\]

Next the \( V_{DS} \) ramp should be supplied. This supply must be able to supply a high current. Therefore a MOS transistor \( M_S \) is connected in series to \( M_{DUT} \). This series MOS transistor is connected to a capacitance \( C_0 \) capable of supplying the high current \( I_D \) with a high current slew rate \( \frac{dI_D}{dt} \) and the charge \( \int_0^T I_D dt \) where \( T \) is the ramp time. The parasitics must be sufficiently small while the capacitance value must be large enough.

For the transfer characteristic, \( I_D \) can be measured potential free using a current probe between the source of \( M_{DUT} \) and \( C_0 \) (fig. 3). As is obvious by the slight decrease of current, self-heating was not completely avoided.

In order to supply the correct control gate voltage to the series MOS transistor corresponding to the \( V_{DS} \) ramp, a regulation circuit was constructed.

**Regulation Circuit**

\( V_{DS} \) is reversed and fed into a high pass filter HP (fig. 4).

\[
V_H = \frac{p \tau_{HP}}{1 + p \tau_{HP}} (-V_{DS}) \tag{5}
\]

\[
p = j2\pi f \tag{6}
\]

\[
\tau_{HP} = R_{HP} C_{HP} \tag{7}
\]

For a frequency below

\[
f_{HP} = \frac{1}{2\pi \tau_{HP}} \tag{8}
\]

the output voltage of the HP is the derivative of \( V_{DS} \).

\[
V_H(f < f_{HP}) \approx p \tau_{HP}(-V_{DS}) \tag{9}
\]

The output voltage of the operational amplifier can be described by

\[
V_{OP} = \frac{V_P - \frac{1}{1+pT} V_E}{\frac{1}{k} + \frac{1}{1+pT}} \tag{10}
\]
Figure 4: Open Loop Frequency Response of the Circuit Components.

\[ k = \frac{V_{OP}}{V_P - V_N} \]

\[ \tau_I = R_I C_I \]

The regulation principle is demonstrated now by removing the high-pass-filter and connecting the output of the low-pass-filter directly to the integrator part \( V_P = V_H \), eqn. 13 to 15.

\[ V_{OP} = \frac{p \tau_H}{1 + p \tau_H} (-V_{DS}) - \frac{1}{R + p \tau_I} V_E \]  

Using an ideal operational amplifier this results in

\[ \lim_{k \to \infty} V_{OP} = \frac{\tau_H (1 + p \tau_I)}{\tau_I (1 + p \tau_H)} (-V_{DS}) - \frac{1}{p \tau_I} V_E \]

Additionally, when choosing the same time constant for \( \tau_{HP} \) and \( \tau_I \)

\[ -V_E = p \tau \left( V_{DS} + \lim_{k \to \infty} V_{OP} \right) \]

\[ \text{Figure 5: Open Loop Frequency Response of the Operational Amplifier and Regulation Circuit.} \]

It can be shown, that the difference between the real derivative \( \frac{dV_{DS}}{dt} \) and the nominal derivative, which is adjusted by \( V_E \), is integrated and fed into the gate of \( M_S \).

So, when \( \frac{dV_{DS}}{dt} \) becomes smaller, the gate voltage of \( M_S \) is rising faster, resulting in a faster pull up of \( V_{DS} \).

In order to keep the deviation from the nominal derivative small, the gain \( F_{MM} = \frac{V_{DS}}{V_{OP}} \) must be as large as possible.

\[ F_{MM} = \frac{g_{m,M_S} (R_{DS} + p L_{o1}) (R_P + p L_{o2})}{(1 + p \tau_R + p \tau_L^2) (R_{DS} + R_P + p L_{o3})} \]  

\[ \tau_R = R_G C_G \]  

\[ \tau_L = L_{o1} C_G \]  

\[ L_{o3} = L_{o1} + L_{o2} + L_{o3} \]

where \( R_{DS} \) is the small signal resistance of \( M_{DUT} \) and \( g_{m,M_S} \) is the gate transconductance, \( R_G \) is the parasitic gate resistance and \( C_G \) is the gate capacitance of \( M_S \). The parallel resistor \( R_P \) is needed for limiting the open loop gain in case of \( M_{DUT} \) saturation. \( L_{o1} \) has no effect, because \( M_S \) is always in saturation.

For the regulation circuit stability, both loops, ending at the positive and the negative input of the operational amplifier, must be considered (fig. 5).

\[ -F_{o,N} = \frac{p \tau_I}{(1 + p \tau_I) \left( \frac{1}{k} - V_{OP} \right)} \]

The Miller-effect is neglected for \( M_S \). Parasitic source induc
tances are neglected generally.

Channel length modulation and gate-drain capacitance of \( M_S \) are neglected.
The stability is mainly affected by the parasitic inductances $L_{o1}$, $L_{o2}$, and $L_{o3}$.

A low-pass-filter is inserted to increase the phase-margin.

\[
\begin{align*}
F_{LP} &= \frac{1}{1 + pr_{LP}} \\
\tau_{LP} &= R_{LP}C_{LP}
\end{align*}
\]

If $M_S$ is switched off too fast at the end of a pulse, then its drain-source voltage may increase above the maximum blocking voltage due to the parasitic inductances. This can be avoided either by limiting the turn off speed or by adding $D$ (transient absorbing Z-diode).

**Input Capacitance**

Fig. 6 shows the measurement circuit for the input capacitance, which is referred to as gate-gate capacitance in this case.

\[
C_{GG} = I_G \frac{dV}{dV_{GS}} \bigg|_{V_{GS} = \text{const}}
\]

Using

\[
C_{GG}(V_{GS}(t), V_{DS}) \approx \tau_D \frac{I_G(t)}{V_D(t)} \bigg|_{V_{GS} = \text{const}}
\]

the result of this measurement is shown in fig. 7. The stability of this circuit is easily achieved without long calculations.

The $L_{o1}$, $L_{o3}$ and $L_{oD}$ (parasitic inductances) and the $R_{o}$ (parasitic resistance) must be as small as possible, because they induce a $V_{DS}$ drop when $I_D$ starts flowing.

![Figure 6: Basic structure of the $C_{GG}$ measurement circuit.](image)

\[
\begin{align*}
-F_{o,P} &= \frac{k(1 + pr_{LP})}{1 + (1 + k)pr_{LP}} \frac{V_P}{F_{LP}} \\
V_P &= F_{LP}F_{MM}(-1)F_{HP}F_{LP} = \frac{V_{OP}}{2}
\end{align*}
\]

The stability is mainly affected by the parasitic inductances $L_{o1}$, $L_{o2}$ and $L_{o3}$.

A low-pass-filter is inserted to increase the phase-margin.

\[
F_{LP} = \frac{1}{1 + pr_{LP}}
\]

\[
\tau_{LP} = R_{LP}C_{LP}
\]

The resistance of the gate current probe has two effects. First this resistance must be considered by adding it to the gate resistance above. Second it causes a drop in the gate current measurement.

The wire of the DUT gate has an $C_{gg}$ (parasitic capacitance) to the ground through the ribbon cable and the case of the gate current probe.

Low pass filters must be inserted between the measurement circuit and the dc voltage sources, because sources typically have parasitic capacitances to ground.

Malfunction usually ends up with destruction of all power semiconductors. Some resistances should be added to the circuits at appropriate nodes in order to achieve a fail-safe behaviour in case of unintentional removal of the pulse generator or an incorrect sequence of connecting and disconnecting the power supplies.

A high $\frac{dV}{dt}$ causes an emission of a magnetic field through the parasitic inductances. In order to keep this influence...
on the measurement result small, the DUT is separated from the $C_0$, $R_P$ and $I_D$ current probe using stacked copper strips insulated with a foil. The regulation and measurement circuit was additionally separated using a ribbon cable. Both, the regulation and measurement circuit and the ribbon cable, are placed in one plane with the main magnetic field lines. The regulation and measurement circuit is shielded by two iron plates. This measurement setup is shown in fig. 8.

Reference