# Gate-Drain Capacitance Behaviour of the DMOS Power Transistor under High Current Flow

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## Abstract

**The gate-drain capacitance of a power DMOS transistor was measured under high current conditions of up to 250 A. Depending on $V_{GS}$ a strong nonlinear characteristic was observed. Using the measured capacitance data the characteristics of the inner MOS transistor and the epi region have been determined separately for parameterisation and modelling.**

## Introduction

The characteristic of the gate-drain capacitance has, due to the *Miller*-effect the most significant influence on the transient behaviour of power DMOS transistors.

This capacitance is normally specified in data sheets without current flow. To our knowledge, it is not yet known how this capacitance behaves under high current. The reason for this is that this cannot easily be determined because of thermal overload and destruction of the device. To avoid this, a circuit has been designed to significantly reduce self-heating.

## Measurement of the Gate Drain Capacitance at High Current Flow

The basic idea is to apply a constant gate voltage $V_{GS}$ and a saw-tooth drain voltage $V_{DS}(t)$ to the device and measuring the gate current $I_G(t)$ (Figure 1). Using the measurement circuit of Figure 2 the gate-drain capacity can be determined by

$$C_{GD}(V_{GS}, V_{DS}(t)) = C\frac{I_G(t)}{I_C(t)}. \qquad (1)$$

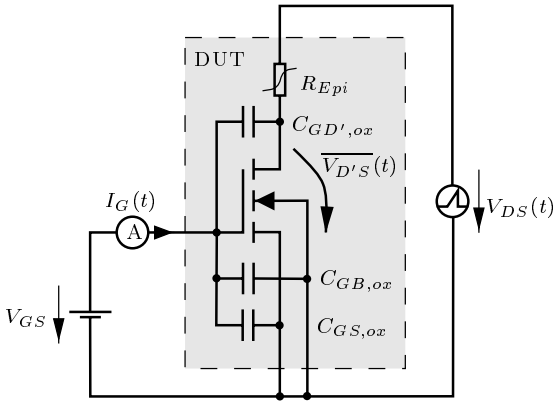


Figure 1: Basic idea of the measurement set-up.

The gate current can be described by

$$\begin{aligned} I_G\Big|_{V_{GS}=const} &\approx -C_{GD',ox}\frac{d\overline{V_{D'S}}}{dt} \\ &= -C_{GD',ox}\frac{d\overline{V_{D'S}}}{dV_{DS}}\frac{dV_{DS}}{dt} \end{aligned} \qquad (2)$$

where $\overline{V_{D'S}}$ is the effective drain voltage of the inner MOS-transistor as shown in Figure 1 which can be determined

$$\overline{V_{D'S}} = \frac{1}{A_{GD',ox}}\int\limits_{A_{GD',ox}} V_{D'S}\,dA \qquad (3)$$

as the average voltage at the surface between gate oxide and $n^-$ epi region (Figure 3).

The gate oxide capacitance (Figure 3) can be divided into the components

$$C_{ox} = C_{GS,ox} + C_{GB,ox} + C_{GD',ox} \qquad (4)$$

overlapping the source, bulk and drain regions of the transistor. $C_{GS,ox}$ is not effected by the changing drain voltage and only to a very small extent

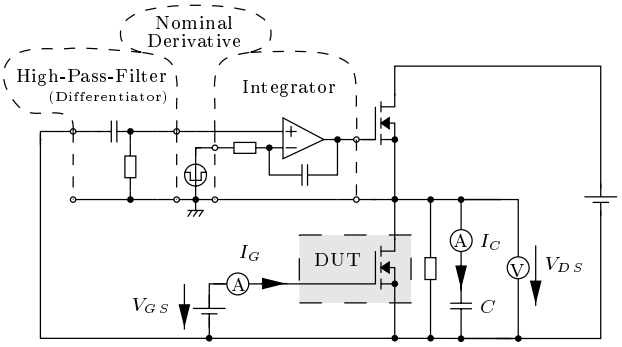


Figure 2: Basic structure of the measurement circuit.

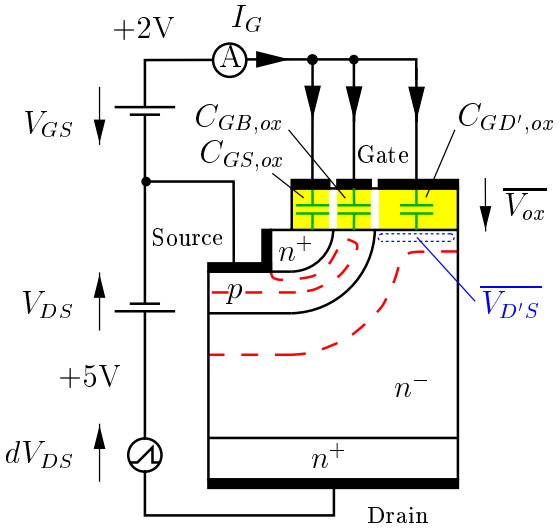


Figure 3: Gate oxide capacitances and effective voltages.

$C_{GB,ox}$. Since furthermore $C_{GD',ox} \gg C_{GB,ox}$ the gate-drain capacitance can be expressed by

$$C_{GD} \approx -C_{GD',ox} \frac{d\overline{V_{D'S}}}{dV_{DS}}\bigg|_{V_{GS}=const} . \qquad (5)$$

With this equation it becomes obvious that the nonliniarity of the gate-drain capacitance is caused by the DC-behaviour of the inner MOS transistor's effective drain voltage $\overline{V_{D'S}}$ in respect to the applied one $V_{DS}$.

Since $\frac{dV_{DS}}{dt}$ is known and the gate current is measured, the capacitance $C_{GD}(V_{GS}, V_{DS})$ (equations 2 and 5)

$$C_{GD} = \frac{I_G}{\frac{dV_{DS}}{dt}}\bigg|_{V_{GS}=const} \qquad (6)$$

can be determined. This has been done for a $\frac{dV_{DS}}{dt}$ of 2 $\frac{\mathrm{V}}{\mu\mathrm{s}}$ and is shown in Figure 4.

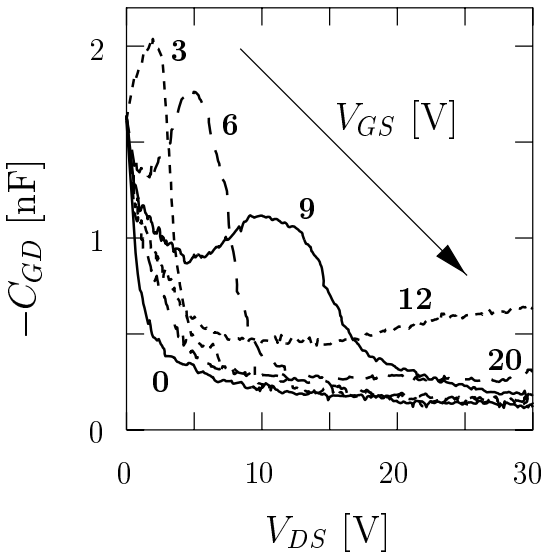


Figure 4: Measured gate-drain capacitance of the BUZ 103 SL.

A strong $V_{GS}$ dependence – this means current dependence – exists. The capacitance behaviour at $V_{GS} = 0\mathrm{V}$ corresponds to the data sheet value. The respective transfer characteristic of the device is shown in Figure 5.

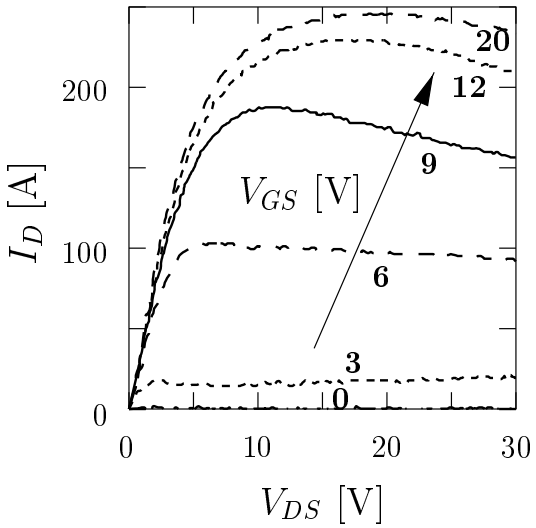


Figure 5: Measured transfer characteristic of the BUZ 103 SL.

As is obvious by the slight decrease in current, self-heating was not completely avoided.

## Validation by Device Simulation

In order to validate the measurements two dimensional device simulations have been performed on the structure of Figure 6.

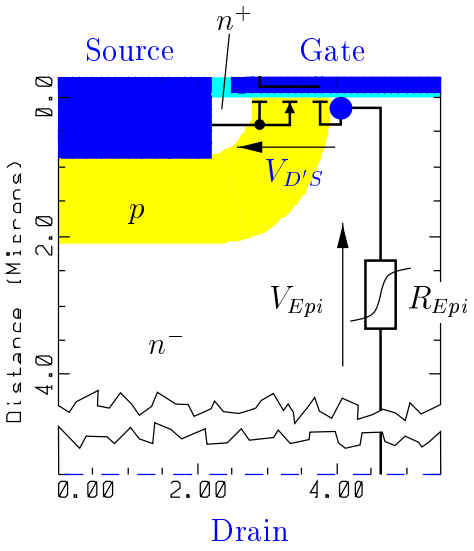


Figure 6: MEDICI structure for device simulation and typical subcircuit model.

The capacitance characteristic could be simulated and verified (Figure 7).

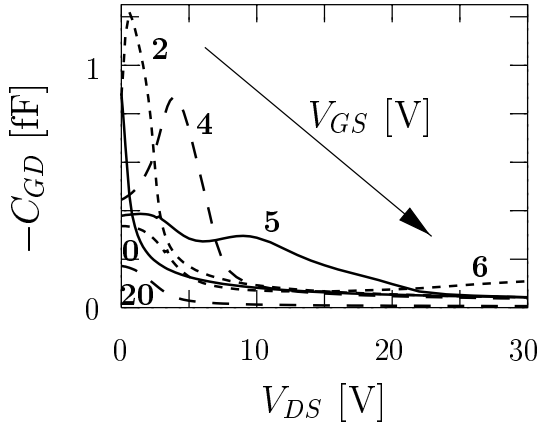


Figure 7: Device simulation of the gate-drain capacitance.

Furthermore it could be verified that the product $C_{GD',ox}\frac{dV_{D'S}}{dV_{DS}}$ (Figure 8) corresponds well with the simulation.

Therefore it can be assumed, that the drain voltage $V_{D'S}$ at the end of the MOS-channel behaves similar to the effective one $\overline{V_{D'S}}$ of Figure 3.

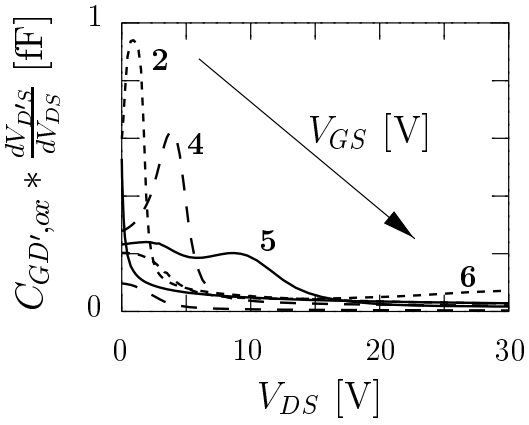


Figure 8: Calculated gate-drain capacitance using $\frac{dV_{D'S}}{dV_{DS}}$ of the device simulation.

## Seperation of MOS and Epi Characteristics

The capacitance $C_{GG}$ is defined by

$$C_{GG} = \left.\frac{I_G}{\frac{dV_{GS}}{dt}}\right|_{V_{DS}=const} . \tag{7}$$

In general the gate current can be described as the displacement current through the gate oxide

$$I_G = C_{ox}\frac{d\overline{V_{ox}}}{dt} \tag{8}$$

where $\overline{V_{ox}}$ denotes the effective oxide voltage which equals the average voltage across the oxide.

$$\overline{V_{ox}} = \frac{1}{A_{ox}}\int_{A_{ox}} V_{ox}\, dA \tag{9}$$

The effective oxide voltage can be approximated by

$$\left. d\overline{V_{ox}}\right|_{V_{DS}=0} \approx \left. d(V_{GS} - \overline{V_{D'S}})\right|_{V_{DS}=0} \tag{10}$$

because this simplification has only a minor effect on equation 13. Equations 7, 8 and 10 result in

$$\left. C_{GG}\right|_{V_{DS}=0} \approx C_{ox}\left(1 - \left.\frac{d\overline{V_{D'S}}}{dV_{GS}}\right|_{V_{DS}=0}\right) . \tag{11}$$

At $V_{GS} = V_{DS} = 0$ the effective drain voltage of the inner MOS-transistor is the sum of the contact voltages from the $n^-$ epi region to the source metal.

$$\left.\overline{V_{D'S}}\right|_{V_{GS}=V_{DS}=0} = \frac{kT}{q}\ln\frac{N_{n^-}}{N_{n^+}} + \phi_{n^+,metal} \tag{12}$$

Starting with these voltages equation 11 is integrated up to $V_{GS}$ while $V_{DS}$ remains zero. Then $V_{GS}$ is held constant and equation 5 is integrated up to $V_{DS}$. This results in

$$\overline{V_{D'S}} \approx -\frac{1}{C_{GD',ox}} \int_0^{V_{DS}} C_{GD}(V_{GS}, V_{DS})\, dV_{DS} + V_{GS} - \frac{1}{C_{ox}} \int_0^{V_{GS}} C_{GG}(V_{GS})\Big|_{V_{DS}=0} dV_{GS} + \overline{V_{D'S}}\Big|_{V_{GS}=V_{DS}=0}. \quad (13)$$

Using the data of the measured capacitance behaviour (Figure 4) the effective drain voltage $\overline{V_{D'S}}$ has been derived by equation 13. Neglecting the contact voltages the result is shown in Figure 9 and correlates well with device simulation [1].

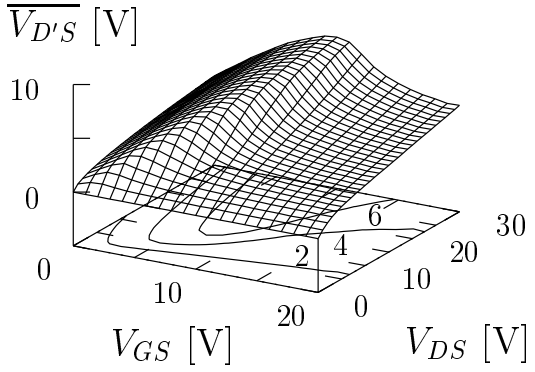


Figure 9: Calculated drain voltage of the inner MOS using the measured data of Figure 4.

Using the data of Figure 9 and the measured transfer characteristic (Figure 5), the inner MOS (Figure 10) and epi (Figure 11) characteristics have been determined separately for parametrisation used in compact circuit models.

## Summary

The gate-drain capacitance of a power DMOS transistor was measured under high current conditions of up to 250 A. Depending on $V_{GS}$ a strong nonlinear characteristic was observed. It has been shown that this characteristic is caused by the DC-behaviour of the inner MOS transistors effective drain voltage $\overline{V_{D'S}}$. Conversely this internal voltage was determined by capacitance measurements. Using the measured capacitance data the characteristics of the inner MOS transistor and the epi region have been determined separately for parameterisation and modelling.

## Reference

[1] C. H. Kreuzer, N. Krischke, P. Nance: Physically Based Description of Quasi-Saturation Region of Vertical DMOS Power Transistors. International Electron Devices Meeting. Technical Digest. IEEE: 1996. Pages 489 - 492.

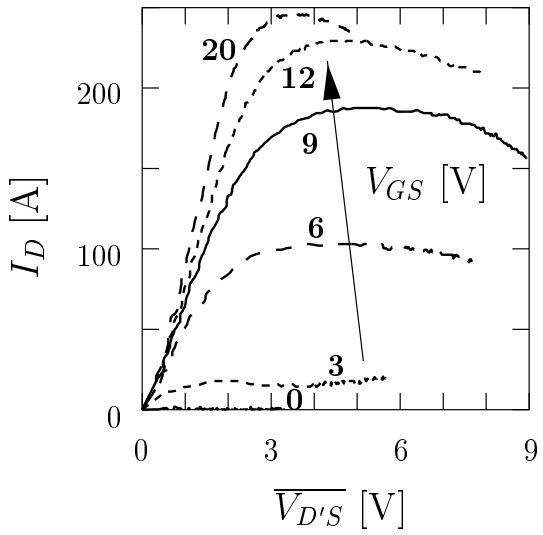


Figure 10: Calculated transfer characteristic of the inner MOS using the measured data of Figure 5 and 9.

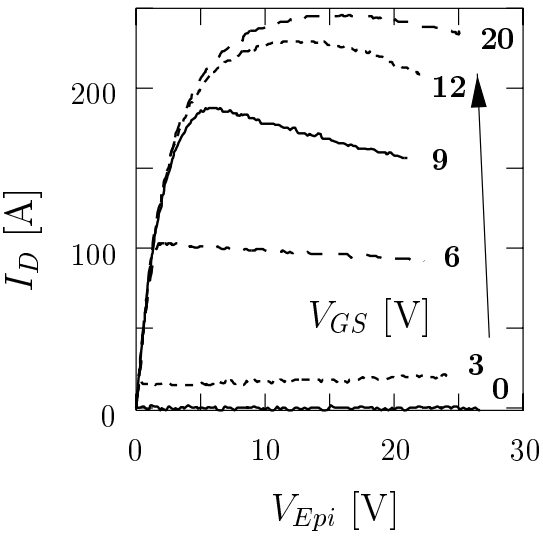


Figure 11: Calculated characteristic of the epi region using the measured data of Figure 5 and 9.