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Fast Simulation Technique for Power Electronic Circuits with Widely Different Time Constants

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Abstract – **A technique for the fast simulation of transients is presented. The method combines the advantages of state space averaging, decoupled simulation and envelope following. It is shown that simulation time can be reduced by a factor between 3 and 10^5 depending on the example without significant reduction of accuracy.**

I. INTRODUCTION

Power electronic circuits usually enclose several widely different time constants. The order of magnitude extends from the switching period with some micro seconds up to seconds and minutes for self-heating. Simulating the dynamics of a system like that with conventional methods is extremely time consuming. In order to solve this problem several approaches were made.

State space averaging in [1] is a method which splits a circuit into a slow and a fast subcircuit. This facilitates, to use different time steps for simulating the two subcircuits and to skip the simulation of several periods of the fast subcircuit. The disadvantage is, that in state space averaging only ideal switching elements can be used. So calculation of switching power losses is impossible.

Another method is decoupled simulation [2], where the fast and the slow subcircuits are linked with a transmission-line model. Unfortunately periods of the fast subcircuit can not be skipped by this method.

Finally, the envelope following method [3] [4] [5] can skip the simulation of several periods efficiently. Since this method does not split the circuit at all it can track only one – the shortest – period of a circuit.

II. FAST SIMULATION TECHNIQUE

In order to combine the advantages of the three methods the circuit is at first partitioned in subcircuits each of them containing only one typical period just like in the decoupled simulation method. Then every subcircuit is simulated in an own simulator process. Finally, the two processes are linked using a new link model, which combines the advantages of the state space averaging method and the envelope following method.

These steps will be demonstrated at a simple circuit.

A. Example

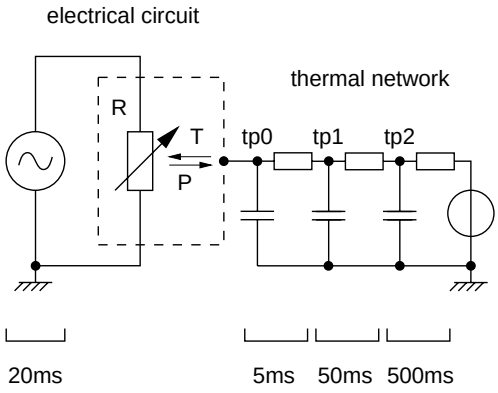

FIGURE 1: CIRCUIT WITH NONLINEAR RESISTOR.

Figure 1 shows a nonlinear resistor

$$R(T) = R_0 * (1 + \frac{1}{K^2}(T - 27°C)^2) \qquad (1)$$

at a sinusoidal voltage source with 50 Hz. The dissipated power is the input size for a thermal network with different time constants.

Initializing all thermal nodes with 27 degree centigrade simulation results in the selfheating curves of Figure 2. It

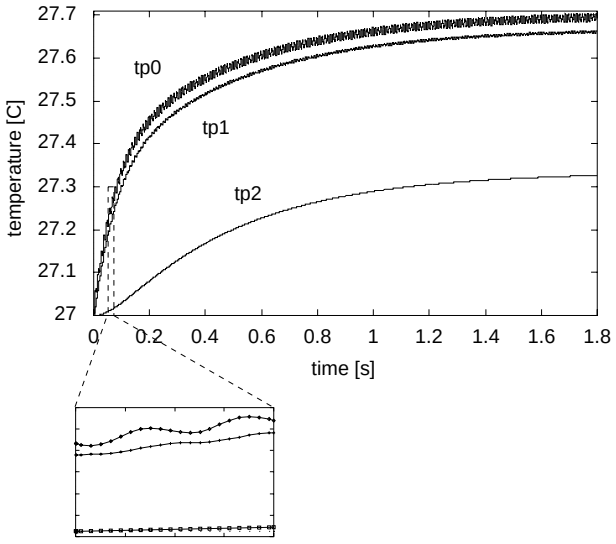

FIGURE 2: CONVENTIONAL SIMULATION.

has to be mentioned that selfheating couples nonlinearely back to the electrical subsystem.

B. Partitioning

It can be recognized that some nodes (tp0, tp1) track the 50 Hz stimulus while tp2 shows a smooth curve because of the big time constant $RC = 500ms \gg 20ms$. This behaviour is given by the circuit. Knowing the behavior of the nodes the circuit can be partitioned in subcircuits each including only nodes with a common speed of changes. Therefore each subcircuit can be simulated seperately with an own time step size resulting in a low computation time for the slow subcircuit.

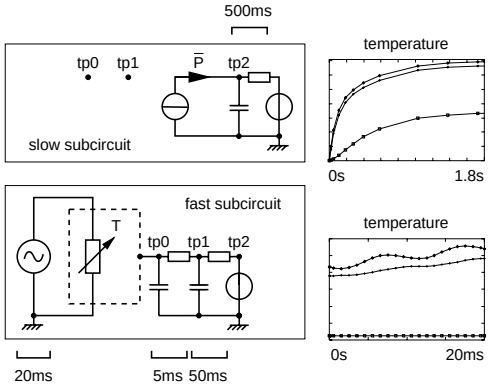

FIGURE 3: PARTITIONING IN SUBCIRCUITS.

Figure 3 shows this partitioning in a slow and a fast subcircuit.

In the fast subcircuit the slow circuit parts are substituted by a single source. Because of the slow thermal changes at this node this thermal source can be set constant during a simulated period.

A single source in the slow subcircuit substitutes the parts of the fast subcircuit. The nodes tp0 and tp1 in the slow subcircuit represent the equivalent nodes of the fast subcircuit sampled at the beginning of every period. This results in smooth curves for tp0 and tp1 too.

Each time a simulation of the fast subcircuit is started, only a single period is simulated. The start time of a period is defined by an event at a node of the fast subcircuit. This event must be unique for every period. In the example the start is indicated by the zero-axis crossing with a positive slope of the electrical node voltage. Modelling this node in the slow subcircuit is omitted, because its value at the time of sampling is known by definiton. Free running circuits can also be simulated using this definition.

C. Linking

The equations of the subcircuits can be solved now by common simulators. Each subcircuit is simulated utilizing an own simulator process. Every subcircuit is missing information about the values of the sampled nodes and the additional sources in the subcircuits. In each case this information can be calculated by the other simulation process. Therefore these simulation processes must be linked (Figure 4).

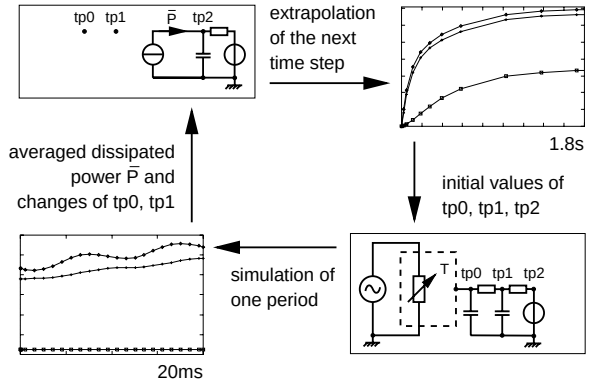

FIGURE 4: LINKING OF SUBCIRCUIT SIMULATION PROCESSES.

At first the slow subcircuit is initialized. Then the fast subcircuit is initialized with the actual values of the slow subcircuit and started. A simulation for one period using a small time step size is started calculating the average dissipated power $\overline{P}$. The changes of tp0, tp1 and the average dissipated power are returned to the simulator with the slow subcircuit. Using this information the next time step of the slow subcircuit is calculated with a large time step size. This process continues till calculation of the curves of the slow

subcircuit is completed.

Generally a circuit with more than two different time constants is partitioned in several subcircuits, which are linked in a tree structure.

The subcircuits are linked at the additional sources utilizing an averaging link model while the sampled nodes are extrapolated. Both procedures will be derived now.

1) Averaging Link Model. A circuit can be cut into fast and slow subcircuits at thermal/electrical capacitors which have a rapidly changing power/current and a slow variing temperature/voltage. Inductors with a fast voltage and slow current can be used too. This model is derived for an electrical capacitor representatively.

The capacitor remains in the slow subcircuit in parallel to an additional current source. An additional voltage source, constant during a simulated period, appears in the fast subcircuit. Both additional sources exchange information. Therefore these sources form a two-port connecting the subcircuits.

The voltage across a capacitor can be described by

$$u(t_n) = \frac{1}{C}\int_{t_l}^{t_n} i(t)dt + u(t_l). \tag{2}$$

If this voltage is only evaluated at discrete times t_i between

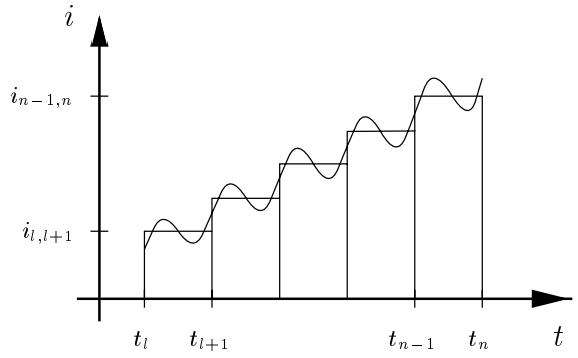

FIGURE 5: AVERAGING AND INTEGRATION.

t_l and t_n the integral of equation 2 can be written as (Figure 5)

$$\int_{t_l}^{t_n} i(t)dt = \sum_{i=l+1}^{n} \int_{t_{i-1}}^{t_i} i(t)dt. \tag{3}$$

Using the current averaged on the intervall (t_i, t_{i-1})

$$i_{i-1,i} = \frac{1}{t_i - t_{i-1}} \int_{t_{i-1}}^{t_i} i(t)dt \tag{4}$$

the integral on the right-hand side of equation 3 is determined by

$$\int_{t_{i-1}}^{t_i} i(t)dt = (t_i - t_{i-1})i_{i-1,i}. \tag{5}$$

Combining equations 2, 3 and 5 results in a description of the capacitor voltage for a series of dicrete times:

$$u(t_n) = \frac{1}{C}\sum_{i=l+1}^{n} (t_i - t_{i-1})i_{i-1,i} + u(t_l). \tag{6}$$

Assume that the actual time of the slow subcircuit is t_m (Figure 6) and the last time step was t_{m-2} then both times are the starting times of the simulation of one period of the fast subcircuit. The endings of these simulated periods are

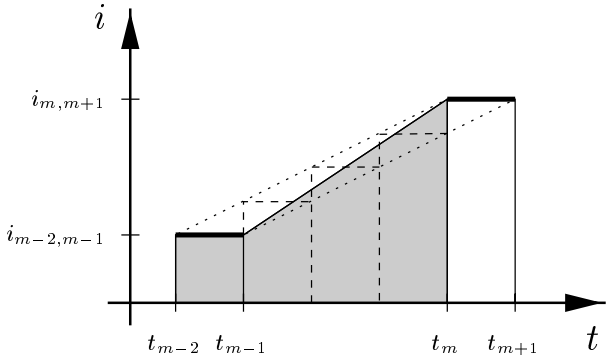

FIGURE 6: INTERPOLATION.

denotetd with t_{m-1} and t_{m+1}. Normally t_{m-1} is separated from t_m by a large time space because of the large time step size used to simulate the slow subcircuit. In order to fill this gap the averaged currents $i_{i-1,i}$ of the missing periods are interpolated linearely[1] and averaged again on the time step size of the slow subcircuit:

$$\begin{aligned} i_{m-2,m} &= [(t_{m-1} - t_{m-2})i_{m-2,m-1} \\ &\quad + (t_m - t_{m-1})\frac{i_{m-2,m-1} + i_{m,m+1}}{2}\Big] \\ &\quad /(t_m - t_{m-2}). \end{aligned} \tag{7}$$

This completes the averaging link model: while simulating a period of the fast subcircuit an additional calculation of the average current through the additional constant voltage source is done using equation 4. At the end of the period the averaged current is submitted to the other simulation process which convertes it by equation 7. If backward euler is used for integrations in the simulation of the slow subcircuit, like equation 3 does, this converted averaged current $i_{m-2,m}$

[1] The time steps of the slow subcircuit need not to be multiples to a period because all curves of the slow subcircuit are smooth and inherent no rapid changes within a period.

can be used directely as the actual current of the additional current source.

If the trapezoidal rule is used, $i_{m-2,m}$ must be transformed. In order to get identical results using the trapezoidal rule instead of backward euler

$$(t_m - t_{m-2})\frac{i^*_{m-4,m-2} + i^*_{m-2,m}}{2} = (t_m - t_{m-2})i_{m-2,m} \tag{8}$$

the transformation can be written as

$$i^*_{m-2,m} = 2i_{m-2,m} - i^*_{m-4,m-2}. \tag{9}$$

The time step size of the slow subcircuit is automaticly restricted by using an implicite integration algorithm in equation 3 if the simulator chooses the time step size in respect to the number of iterations.

2) Extrapolation of Sampled Nodes. All nodes of the fast subcircuit must be initialized prior to a simulation of a period. This is done by the simulator containing the slow subcircuit. Therefore values of sampled nodes must be extrapolated between two time steps using their changes during a period in the fast subcircuit simulation. In order to get reasonable results, the time step size must be restricted appropriately. The best way to achieve this is to use an implicit extrapolation.

A trapezoidal rule based extrapolation (equation 10) produced good results (cp. [3]).

$$\begin{aligned} u_m &= \frac{abu_{m+1} + (2a+b)cu_{m-1} - bcu_{m-2}}{a(b+2c)} \\ a &= t_{m-1} - t_{m-2} \\ b &= t_m - t_{m-1} \\ c &= t_{m+1} - t_m \end{aligned} \tag{10}$$

The assumption of a constant second derivative between two time steps (equation 11; $u_{m-2}, u_{m-1}, u_m, u_{m+1}$ are placed all on a parabola) leads to equivalent precision.

$$\begin{aligned} u_m &= at_m^2 + bt_m + c \\ a &= \frac{u_{m-2} - c - t_{m-2}b}{t_{m-2}^2} \\ b &= \frac{u_{m-1} - \frac{t_{m-1}^2 u_{m-2}}{t_{m-2}^2} - (1 - \frac{t_{m-1}^2}{t_{m-2}^2})c}{t_{m-1} - \frac{t_{m-1}^2}{t_{m-2}}} \\ c &= \frac{u_{m+1} - \frac{t_{m+1}^2 u_{m-2}}{t_{m-2}^2} - d(u_{m-1} - \frac{t_{m-1}^2 u_{m-2}}{t_{m-2}^2})}{1 - \frac{t_{m+1}^2}{t_{m-2}^2} - d(1 - \frac{t_{m-1}^2}{t_{m-2}^2})} \\ d &= \frac{t_{m+1} - \frac{t_{m+1}^2}{t_{m-2}}}{t_{m-1} - \frac{t_{m-1}^2}{t_{m-2}}} \end{aligned} \tag{11}$$

Some values of node states can be calculated at the beginning of a period by performing an DC-analysis on the fast subcircuit or by any other calculations. These nodes need not to be extrapolated and modeld in the slow subcircuit. This reduces simulation time significantly (cp. quasi algebraic variables in [5]).

D. Implementation

The actual implementation utilizes the SABER simulator which makes a large device model library available.

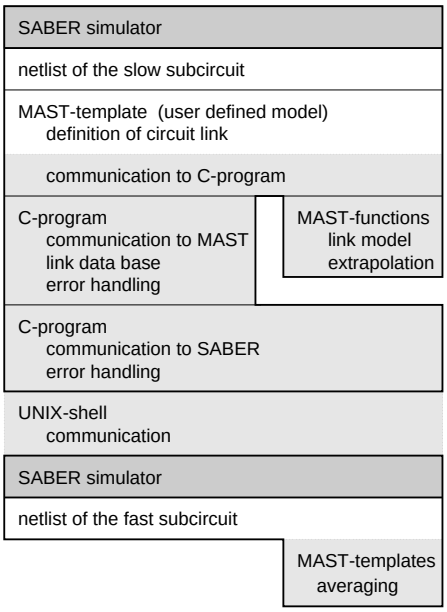

FIGURE 7: IMPLEMENTATION FOR A FAST AND A SLOW SUBCIRCUIT.

Only the white parts in Figure 7 are circuit-specific. Once the light gray parts are programmed the simulator can be started recursively in the needed tree structure.

III. RESULTS

The efficiency and accuracy of the fast simulation technique will be demonstrated for three examples.

1. Example

The selfheating of the nonlinear resistor in Figure 1 was simulated firstly with conventional simulation and secondly with the fast simulation technique. The results are shown in Figure 8. Each simulation point of the fast simulation represents several conventionally simulated periods. Within a region of slow signal changes, two simulation points of the fast simulation are separated by several periods which were not simulated. So the simulation time acceleration depends on the ratio of simulated periods per simulation point and the number of skipped periods. Only 69 simulated periods

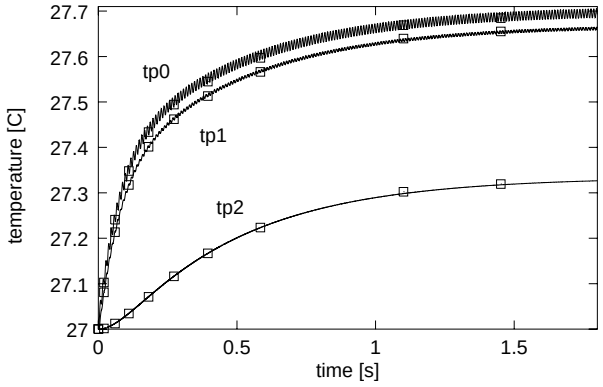

FIGURE 8: TEMPERATURE OF THE THERMAL NODES. — CONVENTIONAL SIMULATION, ⋄ FAST SIMULATION.

were needed for a simulation interval of 5 s resulting in an acceleration factor of 12.2. Another advantage is, that the result of the fast simulation consists of a few data points only. This saves disk space and speeds up storing of the result.

2. Example

The next example in Figure 9 represents a buck converter, which was directly taken from [4].

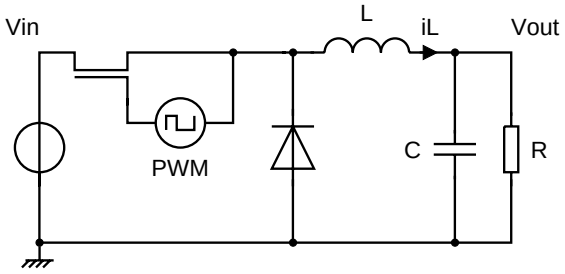

FIGURE 9: BUCK CONVERTER.

Because of the rapid signal changes of V_{out} and i_L (Figures 10 and 11) in the first 0.42 ms the fast simulation can hardly skip periods. In this interval the new simulation technique is approximately as fast as the conventional simulation. For the following interval the computation time is reduced so that the total acceleration factor is 3.38. The maximum error of 1.5% occurs during the fast dynamic behaviour of the signals. Finally, the fast simulation converges to the steady state.

3. Example

At last a complex resonant converter [6] [7] was analysed. In this circuit the Figure of merit $Q = 9.5$ of the resonant

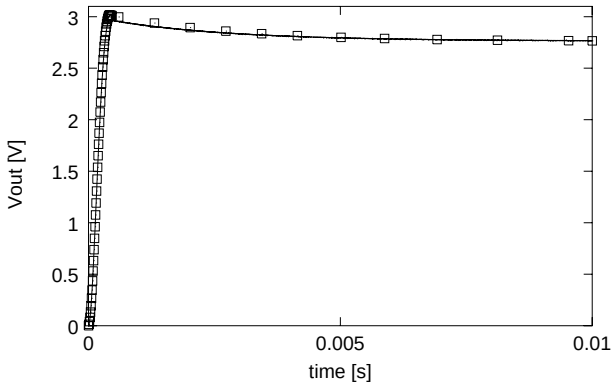

FIGURE 10: V_{out} OF THE BUCK CONVERTER. — CONVENTIONAL SIMULATION, ⋄ FAST SIMULATION.

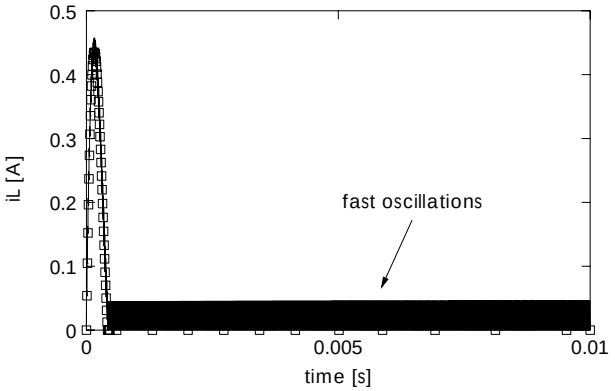

FIGURE 11: i_L OF THE BUCK CONVERTER. — CONVENTIONAL SIMULATION, ⋄ FAST SIMULATION.

load ensures, that the steady state of the electrical circuit is reached after approximately 25 μs (Figure 12).

Using precise device models [8] [9], the power losses of a MOS-FET during switching can be calculated exactly (Figure 13).

This power feeds a thermal network with large time constants from 200 μs up to 20.7 s. The thermal response of the chip temperature is shown in Figure 14.

The self-heating of the MOS-FET changes the behaviour of the device and this couples back to the electrical circuit. In order to evaluate the correct dynamic heating and the steady state, it is necessary to simulate a long time interval (Figure 15). Because of the long computing time, it is impossible to apply conventional simulation.

Table 1 summarizes the simulation results for the three circuits. All simulations were performed using the SABER simulator on a SUN SPARC 20. The first line of each circuit is the result of conventional simulating while the second line shows the fast simulation. CPU Time denotes the computation time which includes storing the result on disk

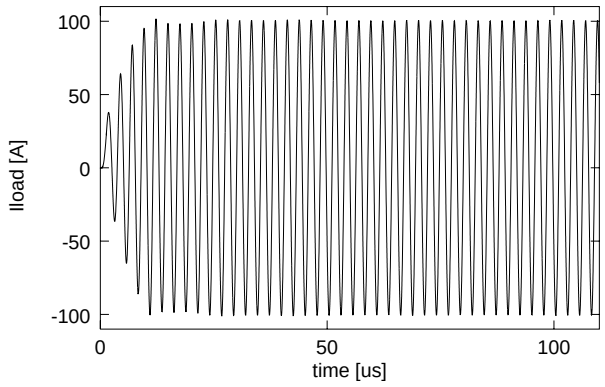

FIGURE 12: CURRENT OF THE LOAD INDUCTOR.

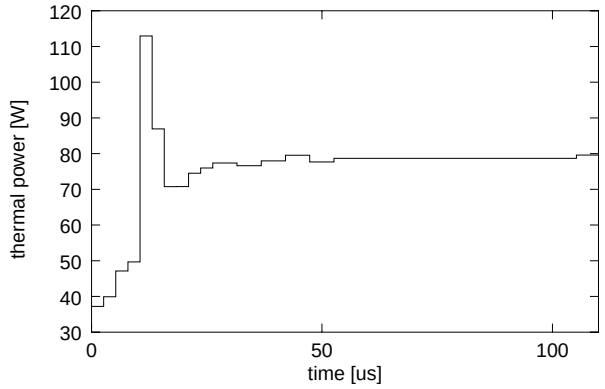

FIGURE 13: AVERAGED DISSIPATED POWER OF A MOS-FET (AVERAGED OVER ONE PERIOD).

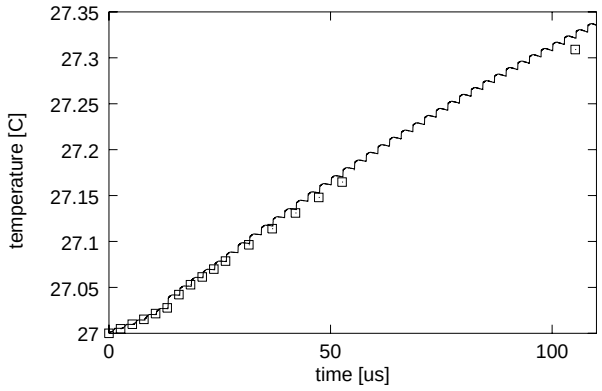

FIGURE 14: CHIP TEMPERATURE OF A MOS-FET. — CONVENTIONAL SIMULATION, ◇ FAST SIMULATION.

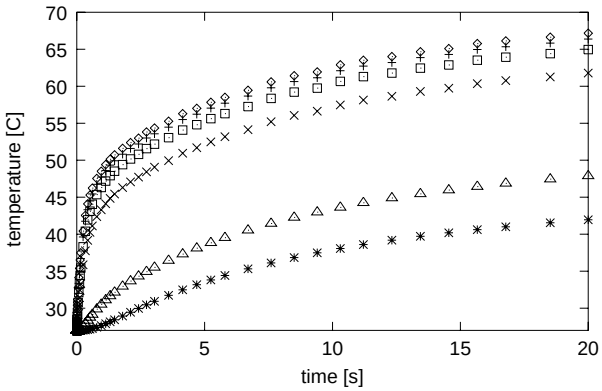

FIGURE 15: TEMPERATURE OF THE THERMAL NODES: FAST SIMULATION.

and excludes the time for communication between the two SABER processes which could be avoided using a specialized simulator. Because of the large simulation time of the conventional simulation the resonant converter was computed only for the first 110 μs. In this example the maximum error was evaluated only in this interval and the CPU time was extrapolated accordingly.

The error of the fast simulation is influenced by the truncation error used which limits the number of skipped periods. Because of that circumstance, there is a trade-off between computation time speed-up and the permitted simulation error.

IV. SUMMARY

A fast simulation technique was introduced, which combines the advantages of the state space averaging method, decoupled simulation and envelope following method. It was shown in some examples that this approach allows the simulation of the transient behaviour of power electronic circuits with widely different time constants. Significant simulation speed-up with a very small simulation error below 4% is possible.

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TABLE 1: SIMULATION RESULTS. FIRST LINE: CONVENTIONAL SIMULATION, SECOND LINE: FAST SIMULATION.

Circuit	Simulated Periods	CPU Time	Acceleration Factor	Max. Error
nonlinear resistor	250 78	188s 15.4s	12.2	— 1.3%
buck converter	1000 108	76.3s 22.6s	3.38	— 1.6%
resonant converter	7.6e6 69	$\approx$ 33a 3.31h	8.7e5	— 3.7%

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